marconi instruments

# TK 1802

## GPIB CONTROLLER

## Instruction Manual

# GPIB CONTROLLER

## TK 1802

Code Nos. 51802-315L
51802-316J
51802-317F
51802-318G

Part No. 46881-465M
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Note ...

Each page bears the date of the original issue or the date and code number of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ .... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

## NOTES AND CAUTIONS

### ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

#### Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

#### Removal of covers

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

#### Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

#### Fuses

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

**CAUTION : STATIC SENSITIVE COMPONENTS**

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed permanently or by repeated discharges.

A low-voltage earthed soldering iron

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

**WARNING : HANDLING HAZARDS**

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

**WARNING : TOXIC HAZARD**

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

# Chapter 1

## GENERAL INFORMATION

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## INTRODUCTION

### General

1. GPIB Controller TK 1802 is designed to control programmable instruments equipped with the General Purpose Interface Bus in accordance with IEEE Standard 488-1978 and IEC Publication 625-1 (First Edition). When fitted with serial line interface boards the instrument also connects to devices operating via EIA Standard RS-423,RS-422,RS-232C or 20 mA current loop.

### Hardware

2. The TK 1802 Controller consists of a main frame, TK 1801/1 plus a front panel containing power on/off and key-operated halt/enable switches. This form of controller is intended for use at stations where operator control is via a visual display unit and keyboard. Where direct operator control of

the instrument is required, GPIB Controller TK 1813 is available which incorporates an operator control panel. Alternatively, Control Panel TK 1803 may be used which is a separate free-standing unit.

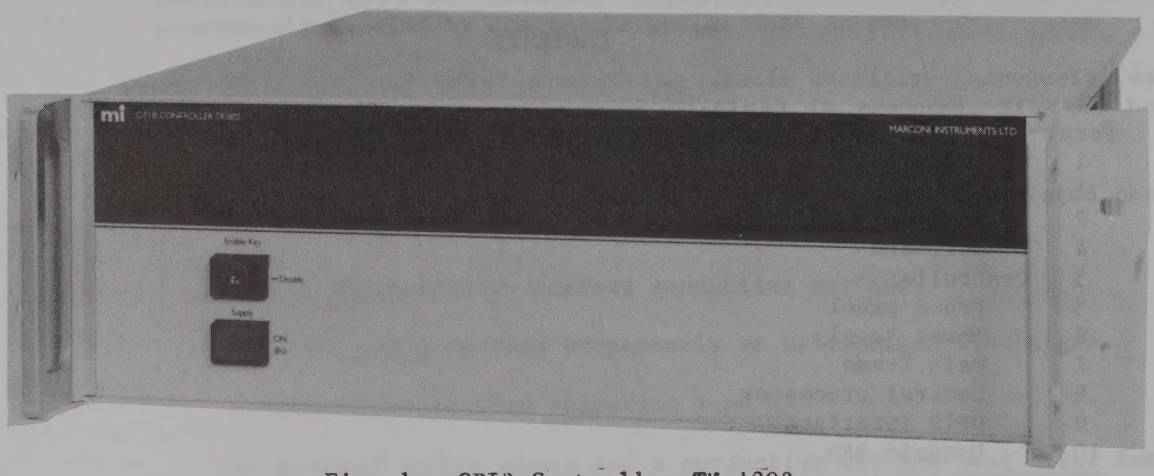


Fig. 1 GPIB Controller TK 1802.

3. Essentially, the main frame consists of a power supply unit plus a backplane and cardframe with a capacity for 8 full-width (quad module) boards. The central processor, which is a DEC LSI-11/23 microcomputer, is a dual module board and together with the GPIB interface IBV11-A and 128 K memory MSV11-LK they take up space for 3 half-width boards. This leaves a further 13 for dual module options. These options include interfaces for v.d.u., line and ticket printers, floppy and Winchester disks. A controller configuration example is shown in Fig. 2.

## Software

4. Each GPIB controller incorporates an in-house developed compiling interpreter which is modular in construction. User programs are written either in INCITE or in an extended basic language, XBASIC, which includes modules tailored to specific requirements. For details refer to the appropriate system's manual.

## CONTROLLER

### Front panel

5. Facilities on the panel are mains on/off and halt/enable. The mains switch not only controls the internal but also external power, via a relay, to a power outlet on the rear panel to which associated equipment may be connected. A key switch is used for the halt/enable control, with the key being removable in both switch positions.

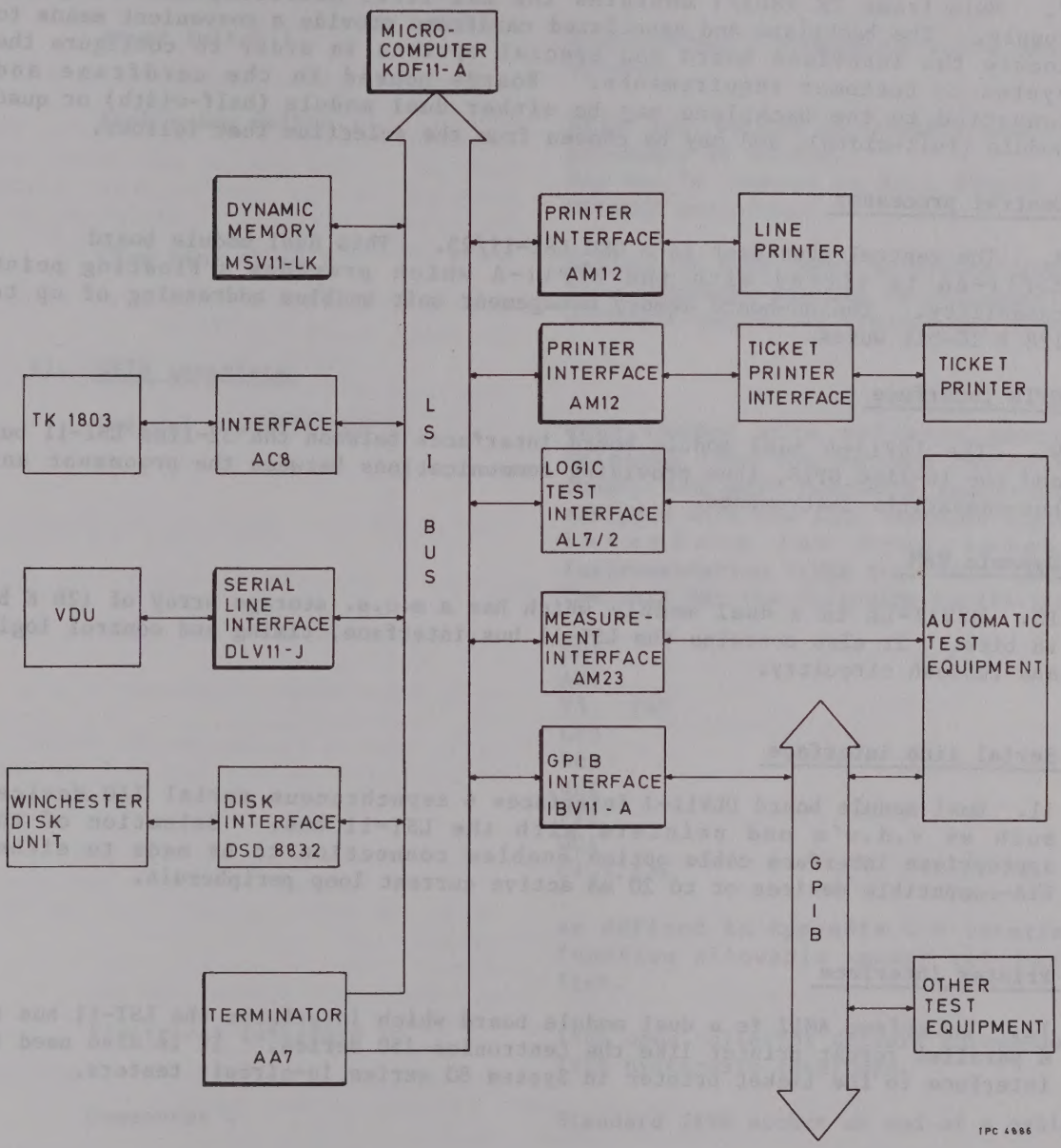


Fig. 2 TK 1802 Controller configuration example showing the relationship between boards and units.

## Power supply

6. DC power for all boards connected to the backplane is generated by regulator circuits within the power supply unit. Control signals to provide correct up-down power sequencing of the processor are also generated as well as line time clock signals.

**Main frame**

7. Main frame TK 1801/1 contains the LSI-11/23 microcomputer and power supply. The backplane and associated cardframe provide a convenient means to locate the interface board and special options in order to configure the system to customer requirements. Boards housed in the cardframe and connected to the backplane may be either dual module (half-width) or quad module (full-width), and may be chosen from the selection that follows.

**Central processor**

8. The central processor is a DEC LSI-11/23. This dual module board KDF11-AA is fitted with the KEF11-A which provides a floating point capability. The on-board memory management unit enables addressing of up to 128 K 16-bit words.

**GPIB interface**

9. The IBV11-A dual module board interfaces between the 32-line LSI-11 bus and the 16-line GPIB, thus providing communications between the processor and bus-compatible instruments.

**Dynamic RAM**

10. MSV11-LK is a dual module which has a m.o.s. storage array of 128 K by 18 bits. It also contains the LSI-11 bus interface, timing and control logic and refresh circuitry.

**Serial line interface**

11. Dual module board DLV11-J interfaces 4 asynchronous serial I/O devices such as v.d.u's and printers with the LSI-11 bus. Selection of the appropriate interface cable option enables connection to be made to either EIA-compatible devices or to 20 mA active current loop peripherals.

**Printer interface**

12. Interface AM12 is a dual module board which interfaces the LSI-11 bus to a parallel format printer like the Centronics 150 series. It is also used to interface to the ticket printer in System 80 series in-circuit testers.

**Terminator AA7**

13. This dual module board correctly terminates the LSI-11 bus.

**Timer/terminator AA7/1**

14. In addition to the LSI-11 bus terminator function, this board also provides a number of timing functions.

**ASSOCIATED EQUIPMENT**

15. Any device having an LSI-11 compatible interface may be plugged into the backplane.

## TK 1802 PERFORMANCE DATA

16. Controls

| | |
|---|---|
| Power switch : | Push-button illuminated white IN-ON, OUT-OFF. |
| Enable key switch : | With key switch in DISABLE position processor is halted.<br>Key may be removed in both ENABLE and DISABLE positions. |
| Line time clock : | Switch on rear panel to enable/disable line frequency signals to processor for software controlled time-of-day clock. |

17. GPIB interface

| | |
|---|---|
| General capabilities : | When loaded with software modules selected from the Marconi Instruments range, the unit controls instruments equipped with the IEEE Standard Digital Interface for Programmable Instrumentation (IEEE Std. 488- 1978). The unit has the following facilities:-<br><br>SH1<br>AH1<br>T5 TE5<br>LE3<br>SR1<br>RL1<br>PP2<br>DC1<br>C1,2,3,4,<br><br>as defined in Appendix C - Interface function allowable subset reference list. |
| Electrical interface : | IEEE open collector drivers throughout.<br>IEEE hysteresis receivers. |
| Connector : | Standard IEEE socket at end of a cable. |
| Additional capabilities : | The unit also complies when structured under 'General Capabilities' with IEC66 (Central Office) 22 Draft when fitted with optional accessory IEC conversion cable. |

18. Central processing unit : DEC LSI-11/23 : Microcomputer fitted with floating point option.

19. Backplane : Standard 22-bit LSI-11 backplane with a total of 8 quad board slots.

20. Ancillaries

| | |
|---|---|
| Cable access : | All cables are accessed underneath removable rear panel |
| Auxiliary supply outlet : | 5 A socket outlet controlled by SUPPLY switch on front panel. The outlet is separately fused in both live and neutral. The outlet and fuses are located on the smaller rear panel. The actual switching is performed by a mains contactor. |
| DC power outlet : | Provides 12 V power which may be used for mains relay operation. |
| 21. Safety regulations : | Complies with IEC 348 and BS 4743 safety requirements. |

22. Limit range of operation

| | |
|---|---|
| Temperature : | $10^0$ to $35^0$ C. |

23. Conditions of storage and transport

| | |
|---|---|
| Temperature : | $-40^0$ C to $+70^0$ C. |
| Humidity : | Up to 90% relative humidity. |
| Altitude : | Up to 2500 m (pressurized freight at 25 kPa differential, i.e. 3.7 $lbf/in^2$). |

24. Power unit

| | |
|---|---|
| Nominal mains voltage range : | 85 to 130 or 170 to 264 V a.c. at 45 to 65 Hz. |
| Consumption : | 1. Internal. Approx. 120 VA. Fused internally.<br>2. Via mains outlet socket 1 kVA max. Fuses on rear panel. |
| Supply lines : | +5 V ±3% 18 A max. backplane load.<br>+12 V ±3% 2.5 A max. backplane load. |
| Short-circuit protection : | Both +5 V and +12 V supply rails have short circuit protection. |

| | |
|---|---|
| Line time clock : | Signals at mains frequency are available and may be patched to the BEVNT L line on the backplane bus for use with software clock routines. |
| Power fail/Automatic restart : | Fault detection and status circuits monitor a.c. and d.c. voltages and generate LSI-11 bus-compatible BPOK H and BDCOK H signals (respectively) to inform modules of power supply status. |
| Fans : | Built-in fans provide cooling for the power supply and modules within the unit. |

25. Dimensions and weight :

| | |
|---|---|
| Height : | 133 mm (5.25 in) |
| Width : | 485 mm (19 in) |
| Depth : | 482 mm (19 in) |
| Weight : | 16.5 kg (36 lb) |

## Alternative versions

26. The following alternative versions of the controller are available :-

| | |
|---|---|
| 51802-315L | Part of OE 1990 Series |
| 51802-316J | Part of OA 1880C |
| 51802-317F | Part of OA 1901C |
| 51802-318G | Part of Workstation 1949 |

## Accessories

27. The accessories listed below are either supplied or optional depending upon the instrument version :-

1. Mains lead, 43129-003W
2. Free plug, 23423-156W
3. GPIB lead assembly, 23435-681X
4. DLV11-J serial line interface, 46662-036J
5. AM12 printer interface, 46883-461V
6. AA7 terminator, 44827-905Z
7. AA7/1 timer/terminator, 46883-550Z
8. AA8 link board, 31828-622Z
9. Quad module extender board, 28541-005U
10. Dual module extender board, 28541-004E
11. AM23 bus measurement interface,44828-897F
12. Instruction manual, H 51801-901R, 46881-465M
13. The GPIB Manual, H 54811-010P, 46881-365R

# Chapter 2

# INSTALLATION

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## PACKING

1. This instrument normally forms part of a system. If the instrument is to be separately returned for servicing, attach a label indicating the service required, type or model number (on rear label), serial number and your return address. Pack the instrument using a strong double-wall carton packed with a 7 to 10 cm layer of shock absorbing material around all sides of the instrument to hold it firmly. Protect the front panel controls with a plywood or cardboard load spreader; if the rear panel has guard plates or other projections a rear load spreader is also advisable.

## POWER SUPPLIES

2. The controller operates on 85 to 130 V and 170 to 264 V a.c. mains, 50 or 60 Hz. Two a.c. supply fuses are fitted in the switch panel located to the rear of the SUPPLY switch. For the 230 V range, the a.c. supply fuses are 1 A and the cooling fans are connected in series. For the 115 V range, the supply fuses are 2 A and the fans are connected in parallel. As supplied, the instrument's power supply is correctly configured for the country of use. However, before switching on, ensure that the instrument is configured for the correct range. To change the range, lift off link SW2 in the power supply unit and replace it in its alternative position. Then configure the fans and change the supply fuses. DC protection is provided by two 5 A fuses for the rear panel SUPPLY OUT socket, and by a 500 mA fuse for the 12 V OUTLET. Ensure

that the power lead from the front panel is connected to the internal switch panel a.c. supply plug marked PLM. Check that the power lead to the rear panel auxiliary power socket is connected to the switch panel socket SKM.

3. The 12 V OUTLET is a 3-pin socket with connections as follows :-

| | |
|---|---|
| Top pin (C) | - +12 V |
| Left-hand pin (B) | - No connection |
| Right-hand pin (A) | - 0 V |

4. When refitting a supply plug to the mains lead note that the wires are colour coded as follows :-

| | | |
|---|---|---|
| Earth (ground) | - | Green/Yellow |
| Neutral | - | Blue |
| Line (phase) | - | Brown |

## Safety testing

5. Where safety tests on the mains input circuit are required, the following procedures can be applied. These comply with BS 4743 and IEC Publication 348. Tests are to be carried out as follows and in the order given, under ambient conditions, to ensure that mains input circuit components and wiring (including earthing) are safe.

(1) Earth lead continuity test from any part of the metal frame to the bared end of the flexible lead for the earth pin of the user's mains plug. Preferably a heavy current (about 25 A) should be applied for not more than 5 seconds.

Test limit : not greater than 0.5 Ω.

(2) 500 V d.c. insulation test from the mains circuit to earth.

Test limit : not less than 2 MΩ.

## INSTALLING BOARDS AND UNITS

### Determining priority

6. The order in which boards (and board units) are installed in the backplane is important. This is because priority is established by the relative positions of the devices along the LSI-11 bus. The board priority may thus be configured by installing modules in appropriate positions in the mainplane. Fig. 1 shows the backplane module locations viewed from the module side. Note that the processor is shown fitted in the top location and must not be fitted in a different location. All other boards may however, be fitted into any available dual option slot. A board with a bus terminator function, such as Terminator AA7 or AA7/1 must occupy the highest numbered position in any configuration.

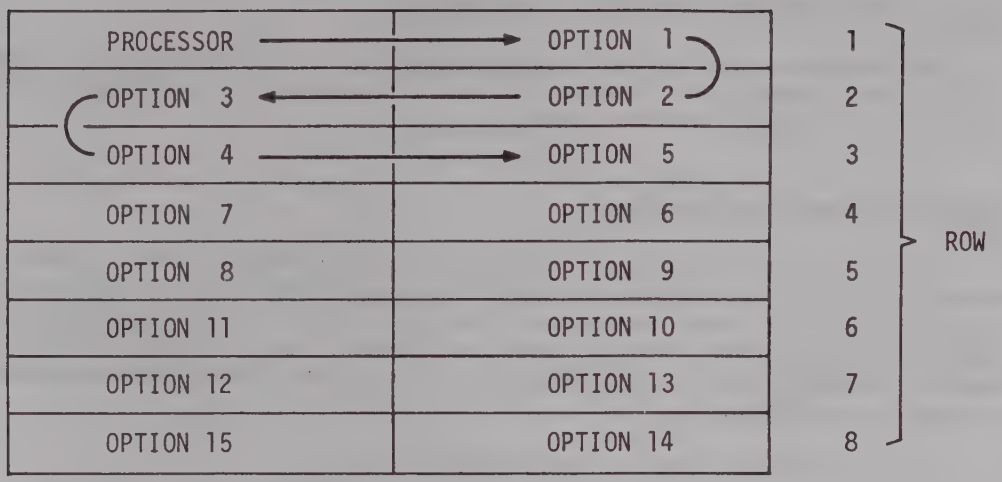


Fig. 1 Backplane processor and option locations viewed from module side. Arrows show interrupt priority sequence for BIAKO L/BIAKI L signals.

## Unused locations

7. The LSI-11 bus structure includes the daisy-chained signals BIAKO L/BIAKI L for interrupts and BDMGI L/BDMGO L for DMA which follow increasing numbered locations. Do not configure the system with unused locations between boards, an unused location will break the daisy-chain signal continuity. To achieve the desired configuration it may be necessary to use link board AA8 which jumpers these signals across the unused slot.

## Inserting and removing boards

8. Modules must be installed or removed only when d.c. power is removed from the backplane. This is accomplished in the controller by switching off the a.c. power by means of the front panel SUPPLY switch.

9. Boards inserted in the backplane are either half-width (dual module) or full-width (quad module). Most boards have handles, and to facilitate removal, all full-width boards additionally have extractors. Boards must be fitted component side uppermost. To ensure correct insertion, all boards have shaped cut-outs on their backplane edges to form fingers which mate with the backplane connector block.

10. Full-width boards have handles which take the form of metal levers. When installing a full-width board carefully start the board fingers into the backplane connector block whilst inserting the metal fingers in the holes provided in the cardframe. Continue by pressing simultaneously on both handles until the board is correctly inserted. Board removal is accomplished by simultaneously pulling on both handles until the handle fingers clear the cardframe when the board can be completely removed.

## EXTERNAL CABLE CONNECTION

### Serial line interface and LSI-11 bus cables

11. The apertures at the bottom of the rear panel are provided to accommodate the LSI-bus ribbon cable as well as up to 4 serial line interface cables used for driving v.d.u's, printers, etc.

### General purpose interface bus

12. The GPIB cable connector at the end of a flying lead allows several connectors to be stacked one on top of another permitting several cables to be connected to the same source and secured by a lockscrew mechanism. This piggy-back arrangement permits star or linear interconnection between the devices forming a system with the restriction that the total cable length for the system must be :

(1) No greater than 20 m (65 ft).

(2) No greater than 2 m (6 ft) times the total number of devices (including the controller) connected to the bus.

The connector contactor assignments are shown in Fig. 2.

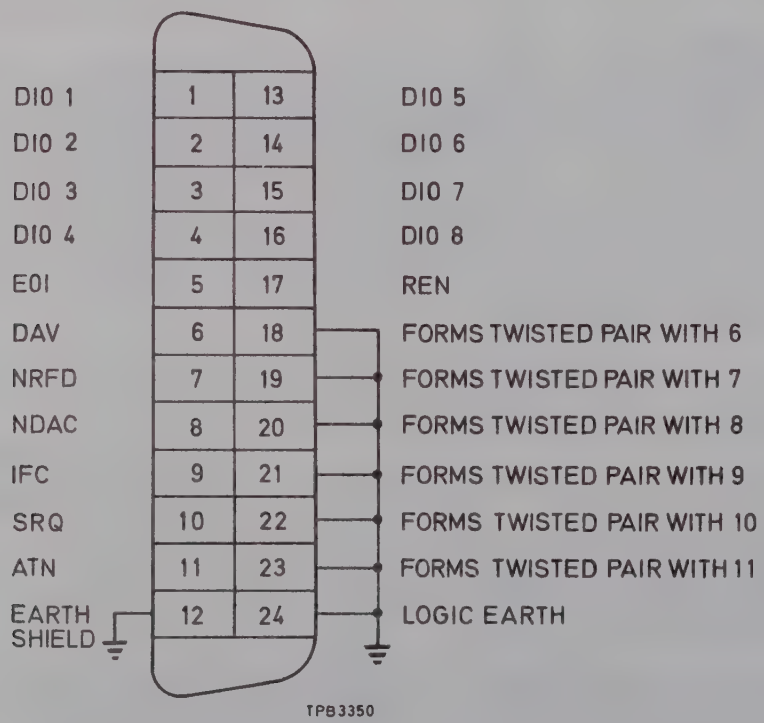


Fig. 2 Interface bus connector contact assignments.

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# OPERATION

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## CONTROLS AND CONNECTORS

### Controller front panel

1. The front panel controls shown in Fig. 1 are as follows :-

(1) SUPPLY switch. Switch ON (button IN) in order to apply power to the controller (fused by internal fuses (14)). Also connects power to the separately-fused (4) rear panel MAINS SUPPLY outlet (8).

(2) ENABLE/DISABLE key switch. Set the key to ENABLE to allow a program to be run. When the key is set to DISABLE the processor is halted. The key may be removed in both the ENABLE and DISABLE positions. Processor operation may also be halted by means of the rocker switch in the power supply unit.

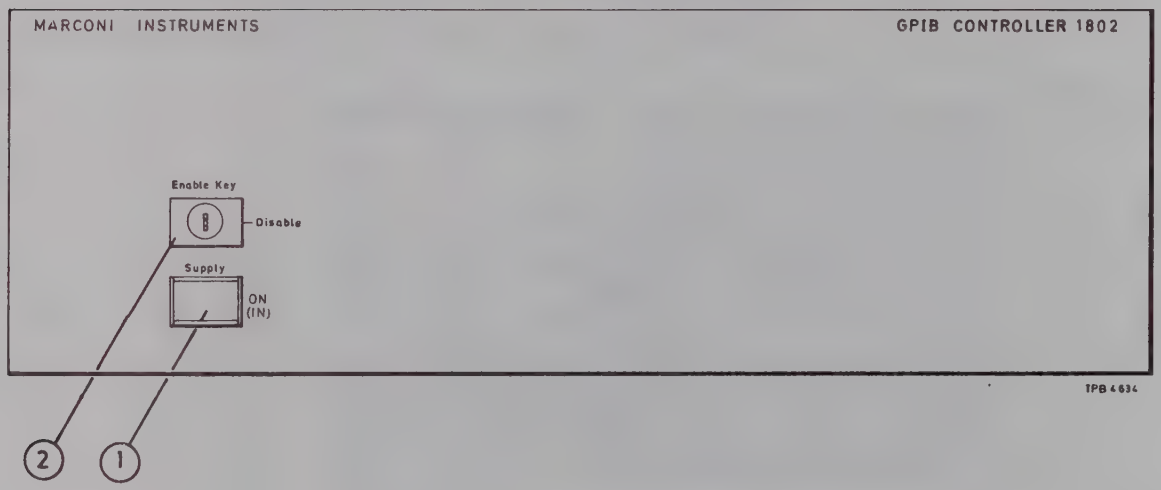


Fig. 1 Front panel controls

### Controller rear panel

2. The rear panel controls and connectors shown in Fig. 2 are as follows :-

(3) Rear panel flap. Pivots at bottom. Open by pulling down using finger aperture after releasing top clips by squeezing them. Panel may be completely removed if desired.

(4) OUTLET FUSES. 5 A quick acting fuses for auxiliary supply to MAINS SUPPLY OUT socket (8).

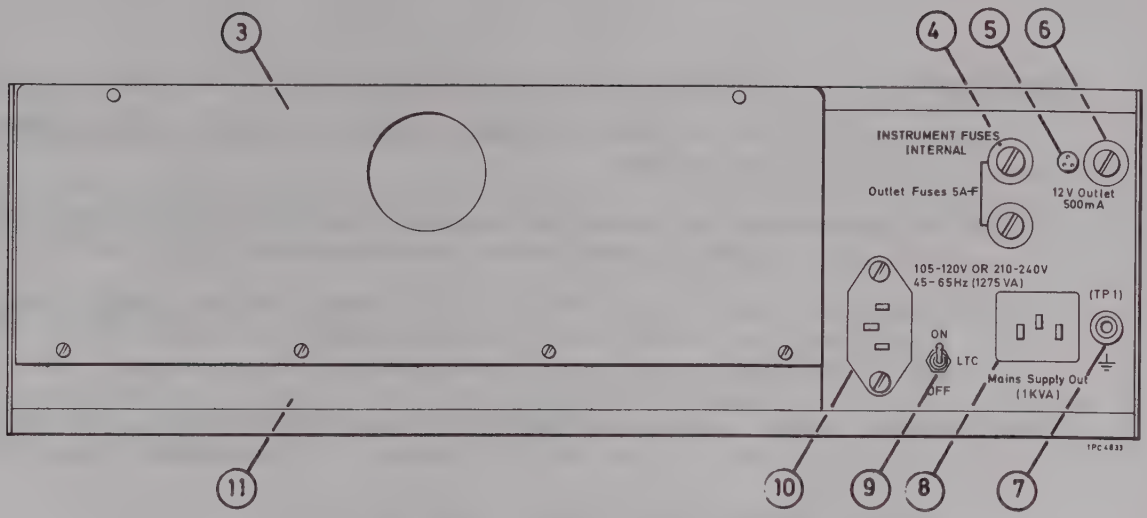


Fig. 2 Rear panel controls and connectors.

(5) 12 V OUTLET. 3-way socket providing 12 V power used typically as coil power for mains relays when current capability of (8) is inadequate. Fused by (6). Connection details are given in Chap. 2.

(6) 12 V OUTLET fuse. 500 mA delay fuse for socket (5).

(7) Earth terminal. 4 mm socket for banana plug.

(8) MAINS SUPPLY OUT socket. Auxiliary supply outlet. May be used to power associated equipment. Controlled by front panel switch (1) and fused by (4).

(9) LTC ON/OFF switch. Selects line time clock at the a.c. power line frequency used by the processor and associated software routines to keep track of correct time of day. LTC operation may also be disabled by a rocker switch within the power unit.

(10) Mains supply in plug. Fused by switch panel fuses (14).

(11) Apertures for serial line interface cables, LSI-11 bus cable and GPIB cable.

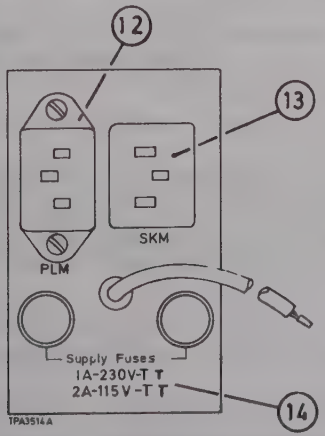


Fig. 3 Switch panel connectors.

Switch panel

3. Mounted to the rear of the front panel SUPPLY switch. The connectors shown in Fig. 3 are as follows:

(12) AC supply plug PLM 3-pin plug used to connect the mains input from the rear mains supply in plug (10) to the front panel SUPPLY switch (1).

(13) Auxiliary supply socket SKM. 3-pin socket used to connect the mains supply from the SUPPLY switch (1) out to the rear panel MAINS SUPPLY OUT socket (8).

(14) SUPPLY FUSES. AC supply fuses for the mains supply in plug (10). 1 A super time delay fuse for 230 V range, 2 A super time delay fuse for 115 V range.

MODULE CONFIGURATIONS

4. Certain modules contain jumpers or switches that are factory configured for specific system applications. This section is intended to make the user aware of features such as, for example, the jumper selected trap and interrupt functions of the processor.

KDF11-AA Processor module (M8186)

5. This dual module board contains 17 jumpers some of which are for user configuration and others which are for test during manufacture and should not be altered. Jumper configurations are listed in Table 1 and the jumper locations are shown in Fig. 4.

Master clock enable (W1)

6. Jumper W1 must always be installed for processor operation. It is provided for manufacturing test purposes and normally should not be removed.

Event line interrupt (W4)

7. Event line interrupt is enabled when W4 is removed and the processor is running. Inserting the jumper disables this feature.

Power-up mode selection (W5,W6)

8. One of the 4 power-up modes shown in Table 1 may be selected by removal or insertion of jumpers W5 and W6. Note that the jumpers do not affect the power-down sequence.

Mode 0: Places the processor in a microcode sequence that fetches the contents of memory locations 24 (program count) and 26 (processor status). Depending on the state of the BHALT signal the processor either enters ODT microcode (BHALT asserted) or begins program execution (BHALT unasserted).

Mode 1: Immediately places the processor in the console ODT microcode regardless of the state of the BHALT signal.

Mode 2: Places processor in a microcode sequence that loads a starting address into PC and begins program execution at this location if BHALT is not asserted. If BHALT is asserted the processor immediately executes the console ODT microcode.

Mode 3: Allows microcode expansion. Not implemented.

**Halt/trap option (W7)**

9. If jumper W7 is installed, a trap to location 10 octal will occur, following a HALT instruction decode. If the jumper is removed, the processor enters console ODT microcode after a HALT instruction.

**Starting address 173000 (W8)**

10. When power-up mode 2 is selected, and jumper W8 is installed as well as a compatible bootstrap such as that of the DSD Winchester interface, program execution begins at address 173000. To select any other starting address this jumper is removed.

TABLE 1 KDF11-AA PROCESSOR MODULE CONFIGURATION SUMMARY

| JUMPER | FUNCTION | ENABLE |
|---|---|---|
| W1 | Master clock - factory configured, do not change | I |
| W2 | Reserved - factory configured, do not change | I |
| W4 | Event line (LTC) interrupt | R |
| W5 & W6 | Power-up mode 0 = PC at 24 and PS at 26 | W5=R W6=R |
| | Power-up mode 1 = ODT microcode | W5=R W6=I |
| | Power-up mode 2 = Generation of bootstrap starting address | W5=I W6=R |
| | Power-up mode 3 = Extended microcode - not used | W5=I W6=I |
| W7 | Halt/trap: Traps to location 10 on halt | I |
| | Halt/trap: Enters console ODT microcode on halt | R |
| W8 | Bootstrap start address 173000 (power-up mode 2 selected) | I |
| | Bootstrap start address user selectable (power-up mode 2 selected) | R |
| W9 to W15 | User selectable bootstrap start address (power-up mode 2 selected) | I='1' R='0' |
| W16 | Reserved - factory configured, do not change | I |
| W17 | Reserved - factory configured, do not change | I |
| W18 | Reserved - factory configured, do not change | I |

I = Installed; R = Removed

**Selectable starting address (W9 to W15)**

11. To start program execution from an address other than 173000 (conventional starting address) when power-up mode 2 is selected, remove W8 and configure the address using W9 to W15. Bits 0 to 8 are set to '0' by the processor, while bits 9 to 15 are set on jumpers W9 to W15 respectively. Jumpers

are installed for logical '1' and removed for logical '0'. The starting address can reside on any 256-word boundary in the lower 32 K of memory address space.

**Standard configuration**

12. W1, W2, W6 and W8 to W18 installed. W4, W5 and W7 removed.

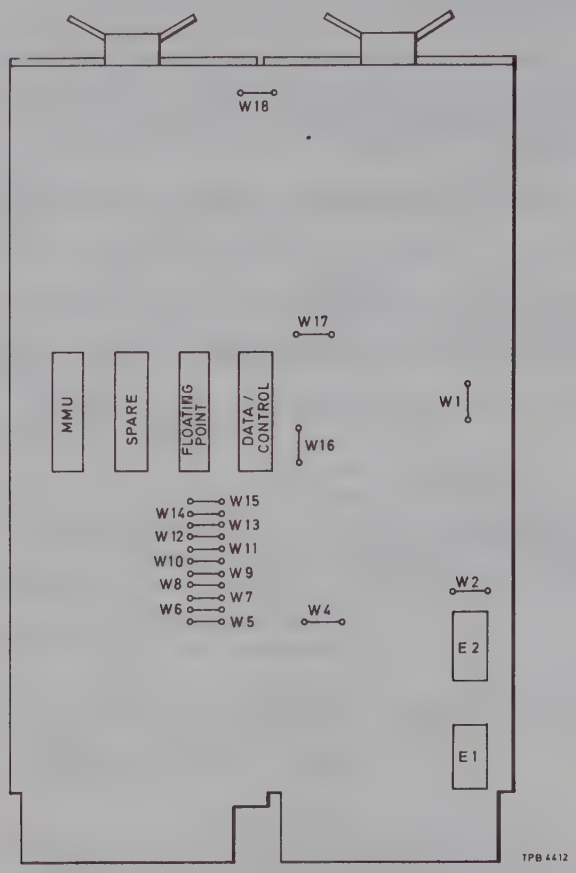


Fig. 4 KDF11-AA jumper locations.

## IBV11-A GPIB interface (M7954)

**General**

13. Dual module board IBV11-A interfaces the LSI-11 bus with the General Purpose Interface Bus (GPIB). It incorporates two switch banks which enable the user to configure the register address and interrupt vector.

**Registers**

14. All communication between the processor and the GPIB board is via the Instrument Bus Status (IBS) and Instrument Bus Data (IBD) registers. The formats are shown in Fig. 6 and are configured using switch bank S2 (for location see Fig. 5). The IBS register is similar in function to other device control and status registers used in DEC equipment (for details of both registers see the Microcomputer Interfaces Handbook).

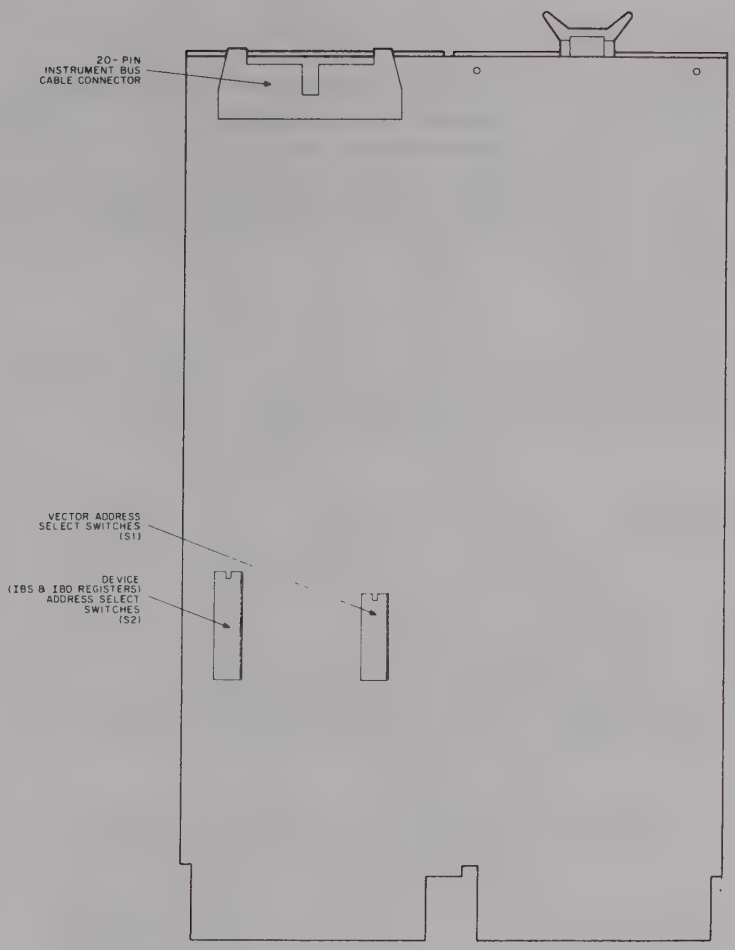


Fig. 5 IBV11-A switch bank locations.

INSTRUMENT BUS STATUS (IBS)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SRQ | ER2 | ER1 | NOT USED | NOT USED | CMP | TKR | LNR | ACC | IE | TON | LON | IBC | REM | EOP | TCS |

INSTRUMENT BUS DATA (IBD)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EOI | ATN | IFC | REN | SRQ | RFD | DAV | DAC | I08 | I07 | I06 | I05 | I04 | I03 | I02 | I01 |

Fig. 6 IBV11-A register word format.

### Register address

15. Only the IBS register address is configurable and it is set on bits 3 to 12 using switches 10 to 1 respectively which form switch bank S2. The IBD register address is equal to the IBS address +2. The method of configuration is shown in Fig. 7. The appropriate switch is set to ON for logical 1. Standard IBS register address used by Marconi Instruments is 171420 octal (IBD address 171422). Address range is 16000X to 17777X (where X represents selection within the module.

### Interrupts

16. The IBV11-A is capable of generating four separate interrupt requests which are priority structured. Interrupts can only be requested when the IBS register IE (interrupt enable) bit is set.

### Interrupt vectors

17. Bits 4 to 8 of the base interrupt vector are set respectively using switches 5 to 1 forming part of switch bank S1 (see Fig. 8). These set the highest priority (error) interrupt vector. Switches 6 and 7 are unused since the associated bits 3 and 2 are internally set to form the remaining three vectors. The vector selected is determined by which bit of the IBS is set (see Table 2). The standard base vector is 420 octal (remaining three vectors, 424, 430 and 434). Base vector range is 300 to 760.

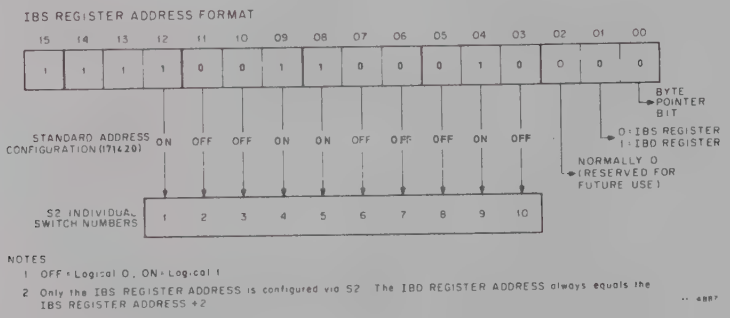
IBS REGISTER ADDRESS FORMAT
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1 1 1 1 0 0 1 1 0 0 0 1 0 0 0 0
BYTE POINTER BIT
0 = IBS REGISTER
1 = IBD REGISTER
NORMALLY 0 (RESERVED FOR FUTURE USE)
STANDARD ADDRESS CONFIGURATION (171420)
ON OFF OFF ON ON OFF OFF OFF ON OFF
S2 INDIVIDUAL SWITCH NUMBERS
1 2 3 4 5 6 7 8 9 10
NOTES
1 OFF = Logical 0, ON = Logical 1
2 Only the IBS REGISTER ADDRESS is configured via S2 The IBD REGISTER ADDRESS always equals the IBS REGISTER ADDRESS +2

Fig. 7 IBV11-A register address format.

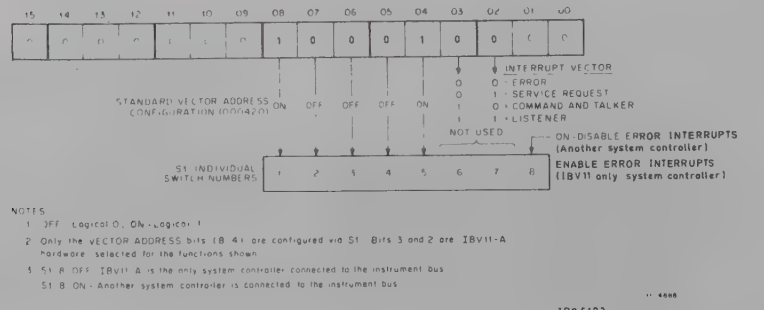
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1 0 0 0 0 1 0 0 0 1 0 0 0 0
INTERRUPT VECTOR
0 0 = ERROR
0 1 = SERVICE REQUEST
1 0 = COMMAND AND TALKER
1 1 = LISTENER
NOT USED
ON = DISABLE ERROR INTERRUPTS (Another system controller)
ENABLE ERROR INTERRUPTS (IBV11 only system controller)
STANDARD VECTOR ADDRESS CONFIGURATION (000420)
ON OFF OFF OFF ON
S1 INDIVIDUAL SWITCH NUMBERS
1 2 3 4 5 6 7 8
NOTES
1 OFF = Logical 0, ON = Logical 1
2 Only the VECTOR ADDRESS bits (8 4) are configured via S1 Bits 3 and 2 are IBV11-A hardware selected for the functions shown
3 S1 8 OFF IBV11 A is the only system controller connected to the instrument bus
S1 8 ON = Another system controller is connected to the instrument bus
TPC 5102

Fig. 8 IBV11-A interrupt vector format.

### System controller

18. When TK 1802 is the only system controller, switch 8 of bank 2 is set to off.

TABLE 2 IBV11-A INTERRUPT VECTORS

| PRIORITY | VECTOR (OCTAL) | IBS REGISTER BIT SET | INTERRUPT |
|---|---|---|---|
| Highest | Configured (N) | ER1, ER2 | Error |
| Second | N+4 | SRQ | Service |
| Third | N+10 | CMD, TKR | Command, Talker |
| Lowest | N+14 | LNR | Listener |

## DLV11-J serial line interface (M8043)

19. As shown in Fig. 9 the DLV11-J module is configured by means of 44 jumpers and 2 resistors to define register addresses, interrupt vectors, data format, baud rates and interface mode.

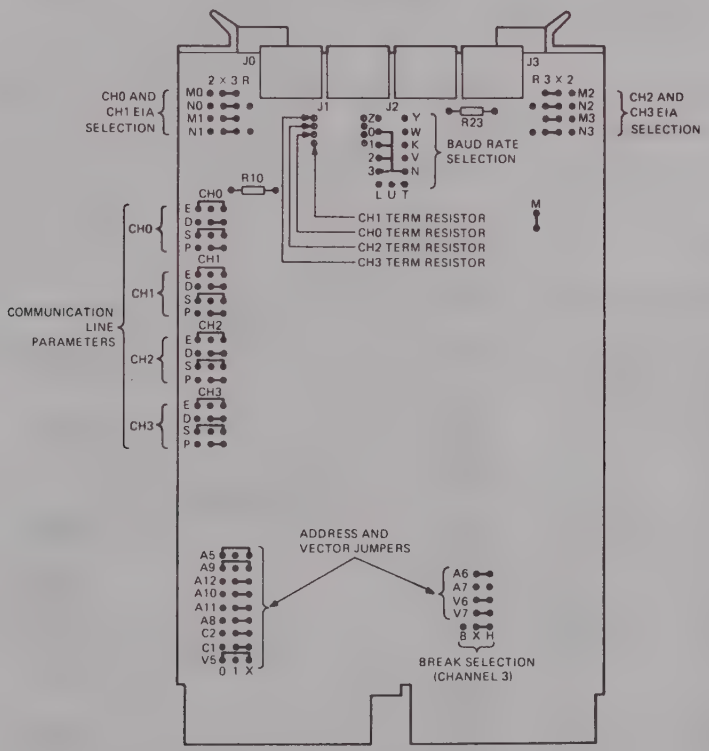


Fig. 9 DLV11-J jumper locations shown configured for OA 1880C.

### Addressing

20. The 18-bit address word is shown in Fig. 10. Bits 5 to 12 are programmed by jumpers. Addresses can range from 160000 to 177770. The address jumpers define the base address (BA), which is the address of the RCSR in the first serial line unit. The addresses of all the other registers for channels 0, 1 and 2 are also defined by the base address (see Table 3). Channel 3 can follow on from the other addresses or it can be selected for driving a console; for the latter, the base address must be 176500, 176540 or 177500.

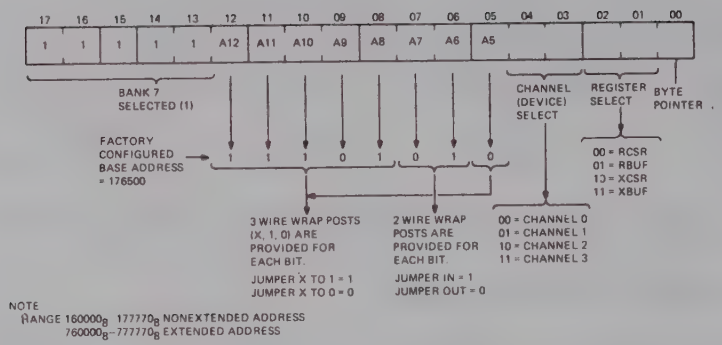
17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1 1 1 1 1 A12 A11 A10 A9 A8 A7 A6 A5
BANK 7 SELECTED (1)
CHANNEL (DEVICE) SELECT
REGISTER SELECT
BYTE POINTER
FACTORY CONFIGURED BASE ADDRESS = 176500
1 1 1 0 1 0 1 0
00 = RCSR
01 = RBUF
10 = XCSR
11 = XBUF
3 WIRE WRAP POSTS (X, 1, 0) ARE PROVIDED FOR EACH BIT.
JUMPER X TO 1 = 1
JUMPER X TO 0 = 0
2 WIRE WRAP POSTS ARE PROVIDED FOR EACH BIT.
JUMPER IN = 1
JUMPER OUT = 0
00 = CHANNEL 0
01 = CHANNEL 1
10 = CHANNEL 2
11 = CHANNEL 3
NOTE
RANGE 160000$_8$ 177770$_8$ NONEXTENDED ADDRESS
760000$_8$-777770$_8$ EXTENDED ADDRESS

Fig. 10 DLV11-J channel 0 RCSR address format.

TABLE 3 DLV11-J ADDRESS ASSIGNMENTS (with console selected)

| Address | Device Register | Associated Vector | |
|---|---|---|---|
| | | Channel 0 | |
| Module Base Address (BA) | RCSR | Module base vector (BV) | |
| BA+2 | RBUF | | |
| BA+4 | XCSR | BV+4 | |
| BA+6 | XBUF | | |
| | | Channel 1 | |
| BA+10 | RCSR | BV+10 | |
| BA+12 | RBUF | | |
| BA+14 | XCSR | BV+14 | |
| BA+16 | XBUF | | |
| | | Channel 2 | |
| BA+20 | RCSR | BV+20 | |
| BA+22 | RBUF | | |
| BA+24 | XCSR | BV+24 | |
| BA+26 | XBUF | | |
| | | Channel 3* | |
| 177560 | RCSR | | |
| 177562 | RBUF | 60 | Console selected |
| 177564 | XCSR | | |
| 177566 | XBUF | 61 | |

*Channel 3 is used as a console device.

### Interrupt vectors

21. The 18-bit interrupt vector is shown in Fig. 11. Bits 5 to 7 are programmed by jumpers. Vector base addresses can be selected from 0 to 377 to define the vectors for all channels (see Table 4).

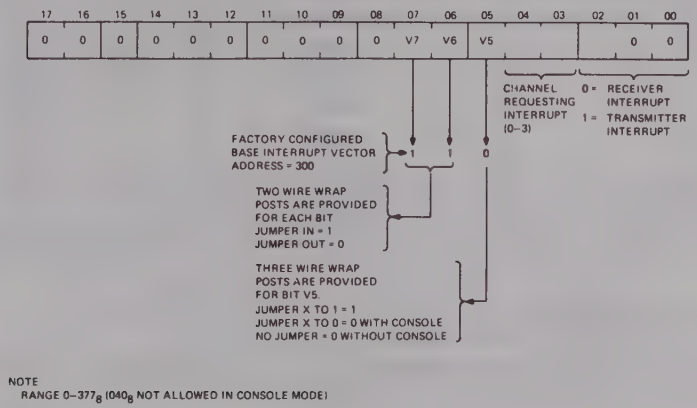
17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
0 0 0 0 0 0 0 0 0 0 V7 V6 V5 0 0
CHANNEL REQUESTING INTERRUPT (0-3)
0 = RECEIVER INTERRUPT
1 = TRANSMITTER INTERRUPT
FACTORY CONFIGURED BASE INTERRUPT VECTOR ADDRESS = 300
1 1 0
TWO WIRE WRAP POSTS ARE PROVIDED FOR EACH BIT
JUMPER IN = 1
JUMPER OUT = 0
THREE WIRE WRAP POSTS ARE PROVIDED FOR BIT V5.
JUMPER X TO 1 = 1
JUMPER X TO 0 = 0 WITH CONSOLE
NO JUMPER = 0 WITHOUT CONSOLE
NOTE
RANGE 0-377$_8$ (040$_8$ NOT ALLOWED IN CONSOLE MODE)

Fig. 11 DLV11-J interrupt vector format.

TABLE 4 DLV11-J VECTOR ASSIGNMENT EXAMPLE (with console selected)

| Standard Address | Interrupt Vector |
|---|---|
| 300 [Module Base Vector (BV)] | Channel 0, receiver |
| 304 (BV+4) | Channel 0, transmitter |
| 310 (BV+10) | Channel 1, receiver |
| 314 (BV+14) | Channel 1, transmitter |
| 320 (BV+20) | Channel 2, receiver |
| 324 (BV+24) | Channel 2, transmitter |
| 60 | Channel 3, receiver |
| 64 Console selected | Channel 3, transmitter |

### Baud rate selection

22. Baud rates can be selected as shown in Table 5 for each channel. Transmit and receive rates are the same.

TABLE 5 DLV11-J BAUD RATE SELECTION

| Jumper label | Baud rate bit/s | RS232C & RS423 slew rate resistor |
|---|---|---|
| U | 150 | 1 MΩ |
| T | 300 | 1 MΩ |
| V | 600 | 1 MΩ |
| W | 1200 | 820 kΩ |
| Y | 2400 | 430 kΩ |
| L | 4800 | 200 kΩ |
| N | 9600 | 120 kΩ |
| K | 19,200 | 51 kΩ |
| Z | 38,400 | 22 kΩ |

**Signal level configuration**

23. For EIA RS232C and RS423 the board is configured as follows (for other configurations see manufacturer's handbook) :-

a) Insert jumpers between pins X and 3 of MO-3 and NO-3.

b) Insert R10 for channels 0 and 1, and R23 for channels 2 and 3 to select slew rate to match baud rate (see Table 5).

**Character format**

24. 7 or 8 data bits, 1 or 2 stop bits, even, odd or no parity may be selected as shown in Table 6.

Table 6 DLV11-J CHARACTER FORMAT JUMPERS

| Label | Channel Parameter | Connection | | Comments |
|---|---|---|---|---|
| | | X to 0 | X to 1 | |
| D | No. of data bits | 7 bits | 8 bits | LSB transmitted first |
| S | No. of stop bits | 1 bit | 2 bits | |
| P | Parity inhibit | Parity generation and detection enabled | Parity bit deleted; parity error = 0 | |
| E* | Even parity enabled* | Odd parity expected | Even parity expected | Only when P =0 |

*Jumper must be installed to 0 or 1 even if no parity is selected.

**Break response (framing error halt) and console selection**

25. Allows entry to console microcode directly from the console device by pressing the BREAK key, producing a framing error. The latter occurs when the received character has no valid stop bit. The BREAK key may demand a bootstrap operation if X is joined to B, or a halt operation if X is joined to H. The latter causes the processor to execute ODT microcode.

26. The BREAK response can only be applied to channel 3 which is the only channel which can be selected for console operation. Console selection requires X to be joined to 1 on C1 and C2. If it is not required, X is joined to 0 on C1 and C2.

▶ Example

27. For the 1924/1 Repair Station using two DLV11-Js, the first is configured as standard and the second is configured as shown in the example forming Table 7. This uses:-

Channel 0 for optional VDU link
Channel 1 for optional VDU link
Channel 2 for Comms link (System 80)
Channel 3 for Comms link (System 80)

**Baud rate patching**

28. The baud rate patching for the various systems is shown in Table 8.

TABLE 7 DLV11-J CONFIGURATION EXAMPLE (for OA 1924/1).

| Label | Jumper | Function implemented |
|---|---|---|
| A12 | X to 1 | |
| A11 | X to 1 | |
| A10 | X to 1 | Base address 176540 for channel 0(J0) |
| A9 | X to 0 | Base address 176550 for channel 1(J1) |
| A8 | X to 1 | Base address 176560 for channel 2(J2) |
| A7 | removed | Base address 176570 for channel 3(J3) |
| A6 | inserted | |
| A5 | X to 1* | |
| C1 | X to 0* | Console not selected |
| C2 | X to 0* | |
| BREAK | XH removed* | No BREAK response |
| V7 | inserted | Base vector 340 for channel 0 |
| V6 | inserted | Base vector 350 for channel 1 |
| V5 | X to 1* | Base vector 360 for channel 2 |
| | | Base vector 370 for channel 3 |
| E | X to 0 | Odd parity |
| D | X to 1 | 8 data bits |
| S | X to 0 | 1 stop bit |
| P | X to 1 | Parity inhibited |

continued ...

TABLE 7 DLV11-J CONFIGURATION EXAMPLE (for OA 1924/1) (continued)

| Label | Jumper | Function implemented |
|---|---|---|
| 0<br>1<br>2<br>3 | | } Baud rate (see Table 8) |
| NO-3<br>MO-3 | X to 3<br>X to 3 | Set for RS232C and RS423<br>signal formats |
| R10<br>R23 | 22 kΩ<br>22 kΩ | Slew rate of 2 µs for channels 0 and 1<br>Slew rate of 2 µs for channels 2 and 3 |

* Changed from factory configuration

TABLE 8 DLV11-J BAUD RATE CONFIGURATION

| System | Board | Channel | Bauds | Jumper |
|---|---|---|---|---|
| System 80 | DLV11J | 0 Comms link | 38.4 kΩ | 0 to Z |
| | | 1 Unused | 9.6 kΩ | 1 to N |
| | | 2 Unused | 9.6 kΩ | 2 to N |
| | | 3 VDU link | 9.6 kΩ | 3 to N |
| Standard Work station | DLV11J/1 | 0 VDU link | 9.6 kΩ | 0 to N |
| | | 1 Comms link | 38.4 kΩ | 1 to Z |
| | | 2 Comms link | 38.4 kΩ | 2 to Z |
| | | 3 Console | 9.6 kΩ | 3 to N |
| | DLV11J/2 | 0 VDU link | 9.6 kΩ | 0 to N |
| | | 1 VDU link | 9.6 kΩ | 1 to N |
| | | 2 Comms link | 38.4 kΩ | 2 to Z |
| | | 3 Comms link | 38.4 kΩ | 3 to Z |
| Standard CAR/Work station | DLV11J/1 | 0 VDU link | 9.6 kΩ | 0 to N |
| | | 1 Comms link | 38.4Ω | 1 to Z |
| | | 2 Digitizer link | 9.6 kΩ | 2 to N |
| | | 3 Console | 9.6 kΩ | 3 to N |
| | DLV11J/2 | 0 VDU link | 9.6 kΩ | 0 to N |
| | | 1 VDU link | 9.6 kΩ | 1 to N |
| | | 2 Comms link | 38.4 kΩ | 2 to Z |
| | | 3 Comms link | 38.4 kΩ | 3 to Z |

## Printer interface AM12

29. As shown in Fig. 12 the AM12 board is configured by means of 17 links to form two consecutive addresses of the form 1YXXX4, 1YXXX6 (where Y = 6 or 7 and X can be any octal digit) and an interrupt vector. Links normally take the form of 2.2 Ω resistors.

### Address

30. The 16-bit address word format is shown in Fig. 13. Bits 3 to 12 of the address in the range 160004 to 177776 octal are programmed by links. For logical '1' the appropriate link is installed.

### Vector

31. The 16-bit interrupt vector format is shown in Fig. 14. Bits 2 to 8 of the vector in the range 0 to 774 octal are programmed by links. For logical '1' the appropriate link is installed.

### Standard patching for ticket printer

32. To select standard addresses 177004/177006 configure the A links as follows :-

| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 |
|---|---|---|---|---|---|---|---|---|---|
| '1' | '1' | '1' | '1' | '0' | '0' | '0' | '0' | '0' | '0' |

33. To select standard vector 274 configure the V links as follows :-

| 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|
| '0' | '1' | '0' | '1' | '1' | '1' | '1' |

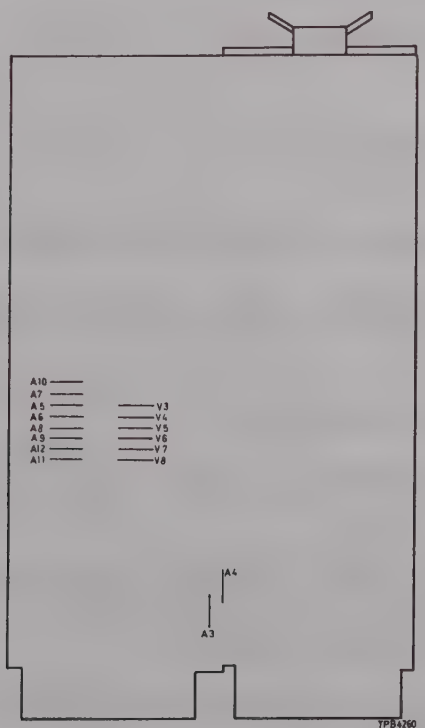


Fig. 12 AM12 link locations.

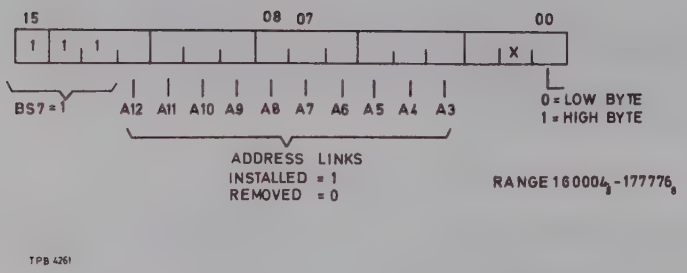


Fig. 13 AM12 address word format.

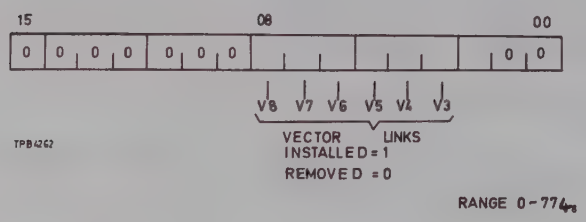


Fig. 14 AM12 interrupt vector format.

**Standard patching for line printer**

34. To select standard addresses 177514/177516 configure the A links as follows :-

| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

35. To select standard vector 200 configure the V links as follows :-

| 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**MSV11-LK Memory module (M8059-KA)**

36. There are four groups of jumpers that alter memory operation. The jumper groups are named as follows :-

Group 1 - General jumpers (Table 9)
Group 2 - Memory starting address jumpers (Table 10)
Group 3 - CSR address jumpers (Table 11)
Group 4 - Power jumpers (Table 12)

Table 13 is a summary of all memory module jumpers. Fig. 15 shows the locations of the jumpers.

TABLE 9 MSV11-LK JUMPERS AND FUNCTIONS (GROUP 1)

| Function type memory | Jumper configuration | Normal Condition |
|---|---|---|
| Non parity | 9 to 10 | out |
| With parity | 11 to 10 | in |
| Parity nonCSR | 18 to 19 | out |
| Parity withCSR | 20 to 19 | in |
| Parity Error Report | | |
| Reported Bad $16^{L}$ NonCSR | 3 to 2 | out |
| Reported Bad $16^{L}$ and BADL 17 with CSR | 1 to 2 | in |
| Write Wrong Parity | | |
| Diagnostic bit for tester use : | | |
| Disable | 8 to 7 | out |
| Enable | 6 to 7 | in |
| CSR Selection | | |
| NonCSR | J to H | out |
| With CSR | F to H | in |
| Peripheral Page Selection | | |
| 2K peripheral page | 29 to 28 | out |
| 4K peripheral page | 27 to 28 | in |
| Full or One-Half Memory Selection | | |
| Half memory selection | 32 to 33 | out |
| Full memory selection | 34 to 33 | in |
| Removal of Lower or Upper Bank (with a Fault) | | |
| Lower bank has failed | 17 to 16 | out |
| Normal operation or upper bank has failed | 15 to 16 | in |
| Extended or Normal Memory Selection | | |
| (Small system) normal operation (128K) | R to T | out |
| (Large system) extended operation (2 meg. words) | R to T | in |

**Starting address**

37. The starting addresses are always on 4 K boundaries and are in two groups :-

(1) First Address of the Range (FAR) - Selects the first address of the 128 K range in which the starting address falls.

(2) Partial Starting Address (PSA) - Selects which 4 K boundary within a 128 K word multiple that the starting address falls.

Note that PSA = MSA - FAR

Configuration example :

A system has 376 K (decimal) bytes. Changing bytes to words, MSA = 188 K.

This address falls in the 128-252 K range as shown in Table 10a. To configure FAR, jumper L to K.

Then PSA = 188 K - 128 K = 60 K. To configure, jumper V,W,X and Y to U (see Table 10b).

**CSR address selection**

38. There are 8 addresses reserved for the CSR register. Every memory module has one CSR register. The module with the lowest starting address should be jumpered for the lowest CSR address using Table 11; the remaining modules will be jumpered in sequence.

**Power jumpers**

39. These allow the memory module to use battery backup power if required (see Table 12).

TABLE 10a MSV11-LK STARTING ADDRESS JUMPERS (GROUP 2)

| Starting address range (FAR) | | Jumpers in (X) to earth (K) | | | | Comments |
|---|---|---|---|---|---|---|
| Decimal (K) | Octal | DAL 21 Pins P | 20 N | 19 M | 18 L | |
| 000-124 | 00000000-00760000 | | | | | Note: To obtain incremental 4 K boundaries within the specified range, repeat wirewrap settings from 0-124 K table. |
| 128-252 | 01000000-01760000 | | | | X | |
| 256-380 | 02000000-02760000 | | | X | | |
| 384-508 | 03000000-03760000 | | | X | X | |
| 512-636 | 04000000-04760000 | | X | | | |
| 040-764 | 05000000-05760000 | | X | | X | |
| 768-892 | 06000000-06760000 | | X | X | | |
| 896-1020 | 07000000-07760000 | | X | X | X | |
| 1024-1148 | 10000000-10760000 | X | | | | |
| 1152-1276 | 11000000-11760000 | X | | | X | |
| 1280-1404 | 12000000-12760000 | X | | X | | |
| 1408-1532 | 13000000-13760000 | X | | X | X | |
| 1536-1660 | 14000000-14760000 | X | X | | | |
| 1664-1788 | 15000000-15760000 | X | X | | X | |
| 1792-1916 | 16000000-16760000 | X | X | X | | |
| 1920-2044 | 17000000-17760000 | X | X | X | X | |

Table 10b MSV11-LK STARTING ADDRESS JUMPERS (GROUP 2)

| Partial starting address (PSA) | | Jumpers in (X) to earth (U) | | | | | Comments |
|---|---|---|---|---|---|---|---|
| Decimal (K) Word | Octal | DAL 17 Pins Z | 16 Y | 15 X | 14 W | 13 V | |
| 0 | 00000000 | | | | | | Note: To obtain any starting address on 4K boundaries from 0-124K, wirewrap daisy chain fashion from pin U which is earthed to each successive pin labelled with X for that address. |
| 4 | 00020000 | | | | | X | |
| 8 | 00040000 | | | | X | | |
| 12 | 00060000 | | | | X | X | |
| 16 | 00100000 | | | X | | | |
| 20 | 00120000 | | | X | | X | |
| 24 | 00140000 | | | X | X | | |
| 28 | 00160000 | | | X | X | X | |
| 32 | 00200000 | | X | | | | |
| 36 | 00220000 | | X | | | X | |
| 40 | 00240000 | | X | | X | | |
| 44 | 00260000 | | X | | X | X | |
| 48 | 00300000 | | X | X | | | |
| 52 | 00320000 | | X | X | | X | |
| 56 | 00340000 | | X | X | X | | |
| 60 | 00360000 | | X | X | X | X | |
| 64 | 00400000 | X | | | | | |
| 68 | 00420000 | X | | | | X | |
| 72 | 00440000 | X | | | X | | |
| 76 | 00460000 | X | | | X | X | |
| 80 | 00500000 | X | | X | | | |
| 84 | 00520000 | X | | X | | X | |
| 88 | 00540000 | X | | X | X | | |
| 92 | 00560000 | X | | X | X | X | |
| 96 | 00600000 | X | X | | | | |
| 100 | 00620000 | X | X | | | X | |
| 104 | 00640000 | X | X | | X | | |
| 108 | 00660000 | X | X | | X | X | |
| 112 | 00700000 | X | X | X | | | |
| 116 | 00720000 | X | X | X | | X | |
| 120 | 00740000 | X | X | X | X | | |
| 124 | 00760000 | X | X | X | X | X | |

TABLE 11 MSV11-LK CSR ADDRESS JUMPERS (GROUP 3)

| 22 Bit CSR Address | 18 Bit CSR Address | C | B | A | Comments |
|---|---|---|---|---|---|
| 17772100 | 772100 | | | | Note: To obtain any 1 of 8 CSR addresses, wirewrap daisy chain fashion from pin E which is earthed to each successive pin labelled X for that address |
| 17772102 | 772102 | | | X | |
| 17772104 | 772104 | | X | | |
| 17772106 | 772106 | | X | X | |
| 17772110 | 772110 | X | | | |
| 17772112 | 772112 | X | | X | |
| 17772114 | 772114 | X | X | | |
| 17772116 | 772116 | X | X | X | |

TABLE 12 MSV11-LK POWER JUMPERS (GROUP 4)

| Voltage connection | Jumper configuration |
|---|---|
| +5 V Non-battery backup | 26 to 25 (W1) |
| +5 Battery backup | 24 to 25 (W2)<br>14 to 13 (W3)*<br>or<br>12 to 13 (W4)* |

*Availability for the +5 V battery backup.

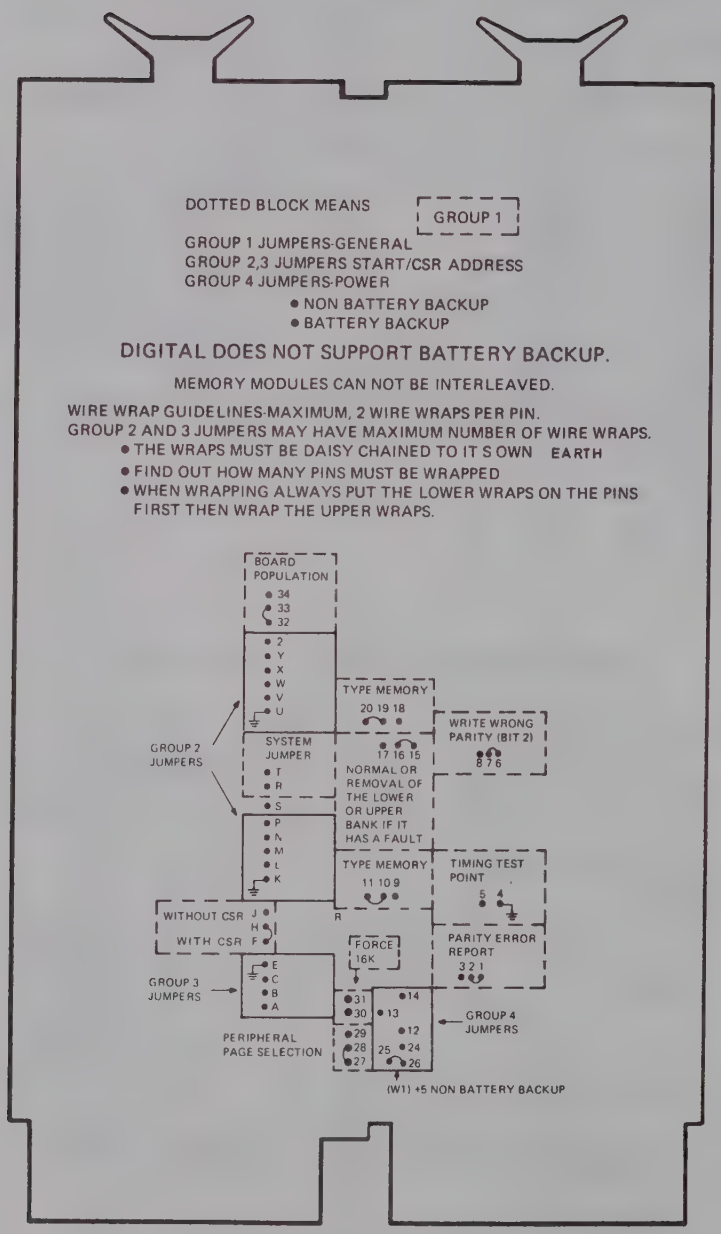


Fig. 15 MSV11-L memory module jumpers.

TABLE 13 MSV11-LK JUMPER CHECK LIST

| Jumper name or Pin to Pin | Jumper in | Jumper out | Wire wrap | Solder | Check |
|---|---|---|---|---|---|
| | General jumpers (Group 1) | | | | |
| 9 to 10 | X | | X | | |
| 11 to 10 | | X | X | | |
| 18 to 19 | | X | X | | |
| 20 to 19 | X | | X | | |
| 3 to 2 | | X | X | | |
| 1 to 2 | X | | X | | |
| 8 to 7 | | X | X | | |
| 6 to 7 | X | | X | | |
| J to H | | X | X | | |
| F to H | X | | X | | |
| 29 to 28 | | X | X | | |
| 27 to 28 | X | | X | | |
| 32 to 33 | | | X | | |
| 34 to 33 | | | X | | |
| 17 to 16 | | X | X | | |
| 15 to 16 | X | | X | | |
| R to T | | X | X | | |
| | Starting address jumpers (Group 2) | | | | |
| P | | X | X | | |
| N | | X | X | | |
| M | | X | X | | |
| L | | X | X | | |
| T | | X | X | | |
| K* | | | | | |
| Z | | X | X | | |
| Y | | X | X | | |
| X | | X | X | | |
| W | | X | X | | |
| V | | X | X | | |
| U* | | | | | |
| | Control and status register jumpers (Group 3) | | | | |
| C | | X | X | | |
| B | | X | X | | |
| A | | X | X | | |
| E* | | | | | |
| | Power jumpers (Group 4) | | | | |
| W1(25 to 26) | X | | | X | |
| W2(24 to 25) | | X | | | |
| W3(13 to 14) | | X | | | |
| W4(12 to 13) | | X | | | |

*Earth

**AA7/1 Timer/terminator**

40. This board is a modified version of the (non-configurable) terminator board AA7. AA7/1 incorporates 5 wire wrap links (for locations see Fig. 16) which are configured as follows :-

L1 - Links in additional 5 V power rail, normally left in place.

L2 - Links line driver to BEVNT line on backplane. When installed, the line time clock control is enabled.

L3 - Links the output of the watchdog timer to the DCOK line on the backplane. Removed only for testing.

L4 - When installed, selects software generated input to the watchdog timer.

L5 - When installed, selects hardware generated input (SRUN) to the watchdog timer.

Note ...

L3 is installed with either L4 or L5. L4 and L5 must not be in place at the same time.

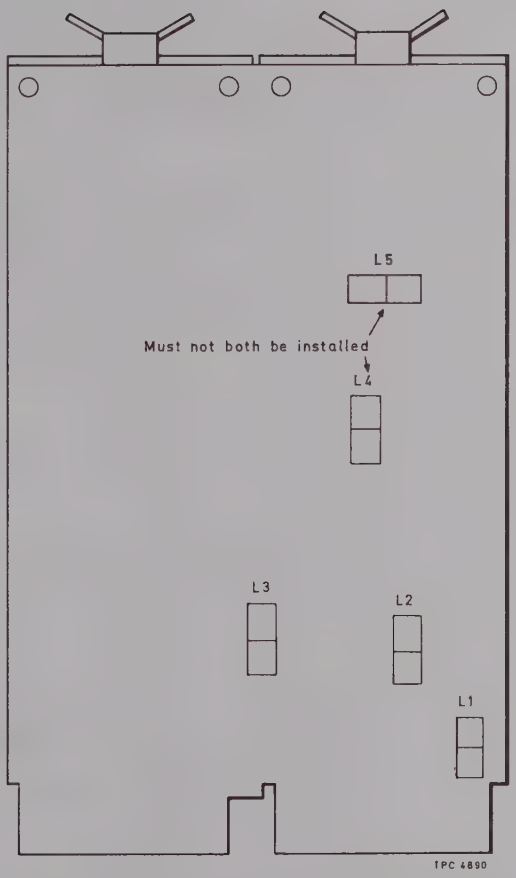


Fig. 16 AA7/1 Timer/terminator link locations.

# Chapter 4

## TECHNICAL DESCRIPTION

CONTENTS


Para.

1 Power supply unit MI/1
1 Input circuit
3 Output circuit
9 Supervisory logic circuit
14 Centronics printer interface board AM12
14 Summary
15 Operation
19 Status registers
20 Timer/terminator board AA7/1
20 Introduction
21 LSI-11 bus terminator
22 Programmable interval timer
24 Watchdog timer
26 Protection register
27 Line time clock control

Fig. Page

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## POWER SUPPLY UNIT MI/1

Circuit diagrams : Chap. 7, Figs. 3 to 6

### Input circuit

1. The mains plug and filter feed the a.c. input to mains transformer T1 and rectifier D20 via thermistor TH1 in the live line and link SW2 in the neutral line. TH1 supplies surge suppression at switch-on while C33 and C35 are initially charging. The link is used to configure the power supply for either the 230 V or the 115 V range. For the 230 V range, D20 acts as a conventional full-wave bridge rectifier feeding to reservoir capacitors C33 and C35 connected in series. For the 115 V range, rectification is supplied using only 2 of the D20 diodes and C33 and C35 are alternately charged so that they form a voltage doubler. Link SW2 also configures centre tapped transformer T1 so as to set the primary/secondary turns ratio to 1:1 and 1:2 for 230 V and 115 V respectively. The T1 centre tapped secondary and full-wave rectifier D3,D4 supply the +ve AUX line providing power for the switched mode control IC in the output circuit. T1 secondary also supplies the AC SENSE signal used to detect incipient power failure by the supervisory logic circuit.

2. The power unit is basically a forward converter. For d.c. to d.c. conversion, the output from D20 is fed to the primary of T2 to be switched by TR10. TR10 is driven by TR1 whose base is connected to the DRIVE line from the switched mode control IC. This IC generates pulses at a constant frequency but of variable duty cycle (the actual mark/space ratio depends on line input and load variations). Power for the driver is supplied via D9 from T2. At switch-on, the +ve AUX line provides the start-up power. T3 couples the driver output to the base of TR3 and isolates the control circuit from the line input. T4 isolates the output from the rectified mains input. When TR10 is conducting energy is passed on the secondaries to the output circuit. Then, after transistor turn-off, the magnetic energy built up in the core of T4 is returned to the d.c. input via the demagnetising winding and diode D22.

## Output circuit

### 5 V d.c. supply

3. Power from the T4 secondary supplying the 5 V d.c. output is rectified by D28,D29 and then smoothed by choke L5 and reservoir capacitor C42. Current limiting protection is provided by IC7 using the CURRENT SENSE output from T5. This is rectified by D23 and fed to potential divider R93,R95 whose junction is connected to IC7 pin 11. If the voltage on this pin exceeds an internal reference, the generation of pulses to the modulator stops so disabling both d.c. supplies.

4. The crowbar circuit at the output protects against an over-voltage condition and comprises Zener diode D26, transistor switch TR12 and s.c.r. TR13. Normally, TR12 is switched off but when the output voltage exceeds the reference set by D26 sufficiently, TR12 switches on. By this action, the gate of TR13 is connected to the junction of R105 and R106 connected across the output. The s.c.r. then switches on so shorting the output. This condition is detected by IC7 on pin 3 and pulse generation is halted.

### Switched mode power supply

5. Primary control of the d.c. output power is exercised by IC7 which is a switched mode control unit operating at approximately 25 kHz. Its functions are to generate pulses to modulate the d.c. input to enable it to be transformed, and to provide power supply protection.

6. The rectified input from T1 on the +VE AUX line feeds to IC7 pin 1 for the internal oscillator and to pin 13 for over-voltage protection. Oscillator operating frequency is determined by R99 and C44 across pins 7 and 8. A stabilized output on pin 2 is fed via potential divider R96 and R97 to pin 6 to set the maximum duty cycle to 40%. The CURRENT SENSE input from T5 to pin 11 enables the output to be cut off should the safe current limit be exceeded. A potential divider formed by R101, R108 and VR5 across the +5 V output controls the gain of the IC.

7. The generated pulsed waveform on the DRIVE line to the base of driver TR1 controls the on-period of modulator TR10 which determines the power supplied to the instrument. If the instrument power consumption increases, the voltage to IC7 pin 3 quickly falls. Comparison with an internal reference results in a decreased output pulse width. This changes TR10 on period so that more energy is drawn from T2/T4 until the voltage on pin 3 IC7 accords with that of the reference. For a decrease in the power consumption a similar but opposite operation is performed.

**12 V d.c. supply**

8. Power from the T4 secondary supplying the 12 V d.c. output is rectified by D15,D16 and then smoothed by chokes L1 and L2 and reservoir capacitors C27 and C47. Regulation is by IC6 whose input is clamped to 20 V by Zener diode D10. IC6 output on pin 11 provides the base drive for series pass transistor TR9. Short circuit protection is provided by R76 connected to pin 3. When the current through this resistor exceeds a safe value the drive to TR9 is removed interrupting the supply. The output voltage is sampled at pin 4 which is connected to the junction of R64 and R65 which, together with VR4, form a potential divider across the output. By this means changes in the output voltage are detected and the drive to TR9 adjusted to restore the voltage to its correct value. Pin 8 is connected to the circuit based on transistor switch TR6 and Zener diode D13. Normally, TR6 is switched on connecting pin 8 to earth, but if a short circuit occurs in the 5 V supply TR6 switches off causing IC6 to shut down. The 12 V output is over-voltage protected in a similar manner to the 5 V supply. When a high voltage occurs, TR7 is forward biased and switches on. This causes s.c.r. TR8 to also switch on which shorts the output to earth.

**Supervisory logic circuit**

**DCOK sensing circuit**

9. The supervisory logic circuit is summarized in Fig. 1. +5 V from the output circuit is applied to IC1 pin 5 non-inverting input and compared with a reference on pin 4. The value of this reference voltage is determined by Zener diode D8 and the potential divider formed by R10 and R11. When the compared voltage exceeds the reference, a high is applied via an inverter to a l.e.d. which illuminates to indicate +5VOK. The regulated +12 V from the output circuit is similarly monitored by comparator IC1 on pin 7 and, during normal operation, a l.e.d. illuminates to indicate +12 VOK. Outputs from the two comparators are taken to an AND gate and, providing ACOK is indicated, electronic switch TR3 is held off causing the associated pull-up resistor to assert DCOK by taking the BDCOK line high. Should either d.c. supply fail, the resulting low comparator output indicates the fault condition by extinguishing the +5VOK or +12VOK l.e.d. and switching TR3 on to take the BDCOK line low.

**POK sensing circuit**

10. This circuit monitors the a.c. supply to detect the change in mains frequency indicating the onset of power failure. Transformer T1 secondary winding is connected via AC SENSE diodes D1 and D2 to comparator IC1 pin 11. This input, at twice the mains frequency, is compared with a reference voltage and the pulsed output is used to drive a retriggerable monostable. If the a.c. power is satisfactory (and providing the d.c. power supplies are also normal) the IC is continuously retriggered to provide constant signal outputs. This is due to the monostable on-period of 15 ms being greater than the period of the input waveform and the effect of C17 and C18. The monostable Q output causes the ACOK l.e.d. to illuminate while the Q output to the inverting pin 8 of comparator IC1 causes transistor switch TR4 to be held off. The associated pull-up resistor takes the BPOK line high to assert POK. Should the power start to fail, the monostable retriggering frequency decreases so that the fault condition is indicated by C17 and C18 discharging to extinguish the ACOK l.e.d. and to switch TR4 on to take the BPOK line low. If this occurs during processor operation, a power fail trap sequence is initiated.

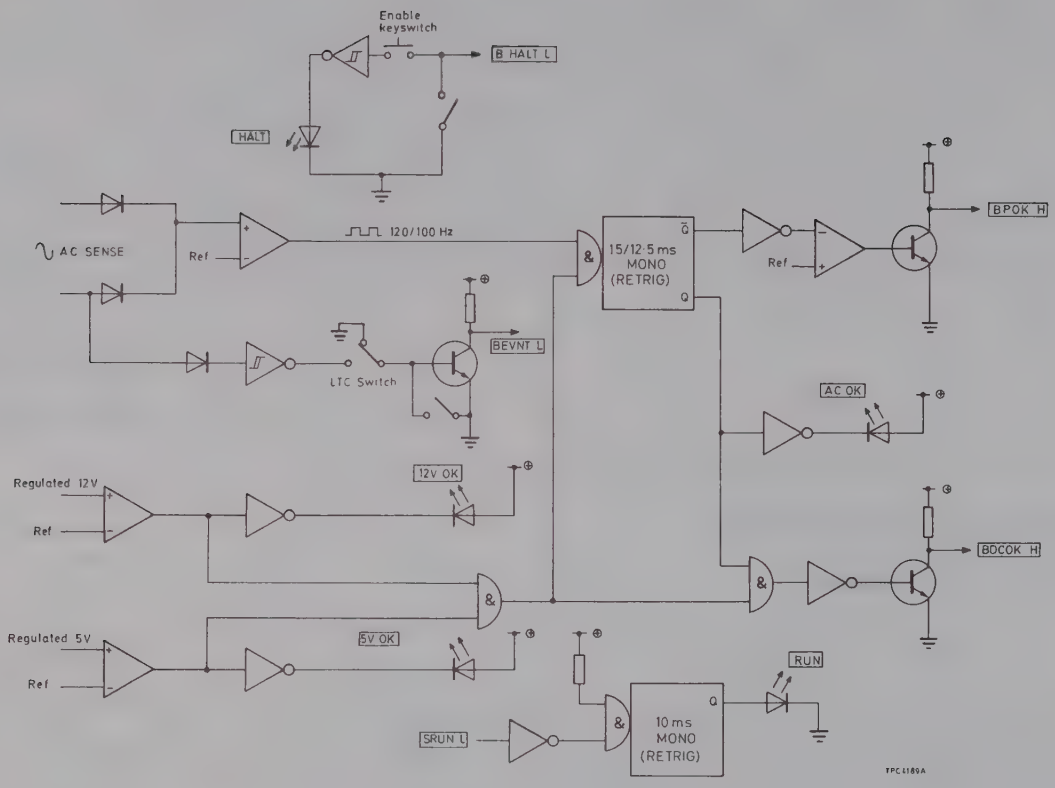



Fig. 1 Supervisory logic circuit summary.

**Event clock generator**

11. To supply line time clock signals, an input from mains transformer T4 secondary is taken via diode D7 to a Schmitt inverter. Providing the rear panel LTC switch is in the ON position and the LINE TIME CLOCK ENABLE switch is open, transistor switch TR5 pulses the BEVNT line low at the line rate. The timing signals may be used to cause a line time clock interrupt by means of a software routine. The processor may use the timing signals to define time intervals in multiples of the line time period.

**RUN sensing circuit**

12. Whenever the microcomputer is executing a program, the SRUN signal input to the board is active and consists of a series of pulses. The pulses trigger a 10 ms monostable on each pulse leading edge so keeping it retriggered. The Q output on pin 4 causes an l.e.d. to illuminate to indicate the RUN condition. When the microcomputer is in the HALT mode the SRUN pulses cease causing the monostable to reset after a 10 ms delay and the RUN indicator is extinguished.

**HALT enable**

13. Whenever the microcomputer is not executing a program, HALT is asserted by the processor taking the BHALT line low. HALT may be asserted manually by the front panel ENABLE keyswitch or by the HALT/ENABLE switch. In either case, Schmitt inverters are triggered to cause an l.e.d. to illuminate to indicate the HALT condition.

## CENTRONICS PRINTER INTERFACE BOARD AM12

Circuit diagram : Chap. 7, Fig. 6

### Summary

14. This board is addressed by the computer to implement the LSI-11 bus protocol and to receive 7-bit ISO characters for onward transmission to a line or ticket printer.

### Operation

15. Transceivers IC1 to IC4 monitor the LSI-11 bus to identify the board address. When the address configured by the links to the JA inputs matches the logic on the BDAL 3 to 12 lines when BBS7 is asserted, the MATCH outputs go high. This latches ENB into IC6 which manages the bus protocol. Bits 1 and 2 of the address on the BDAL 1 and 2 lines are decoded by IC6 to latch one of the SEL0, 2,4 or 6 lines when BSYNC is asserted. IC6 also monitors the state of the BDIN and BDOUT lines to determine the subsequent type of data transfer (DATI or DATO). Data is received from the bus when IC6 sets the transceivers' REC inputs high and the XMIT inputs low. The data representing the character to be printed is applied in ASCII form to latch IC11.

16. When a previous character has been printed, an ACKNLG pulse clocks latch IC13 and providing that no fault is present to hold IC15 pin 13 low, RQSTB is asserted at pin 15 of interrupt chip IC5. When the processor responds, it sends new data to the transceivers (except to IC2 which is not used for this purpose) and causes OUTLB to go low from IC6. OUTLB is ANDed with the previously latched SEL6 and used to clock the data from IC11 via buffer IC14 to the printer. Monostable IC8 is also clocked which remains on for 1.5 µs. The $\bar{Q}$ output resets the ACKNLG latch IC13 while the Q output triggers a further monostable. IC8 $\bar{Q}$ output on pin 12 produces the 1.5 µs STROBE pulse to allow the printing of the selected character.

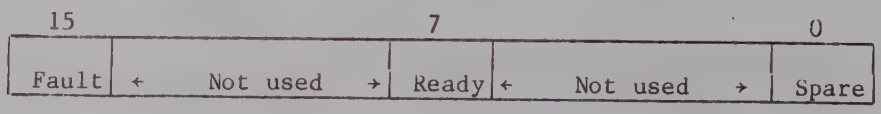
17. When RQST is asserted to IC5 it, in turn, asserts BIRQ in order to request a processor interrupt. When the request is granted, the processor asserts BDIN. IC5 then takes VECTOR high to the transceivers which respond by gating the device vector, configured by the links on the JV inputs, directly onto the bus.

18. To enable the processor to read control and status register (CSR) IC9, INWD and SEL4 are both asserted low by IC6. These signals are ANDed by IC12 causing pin 1 to go high. Tristate IC9 is enabled to place the status word on the data lines while XMIT is taken high to enable transceiver IC3 to transfer the word out onto the LSI-11 bus.

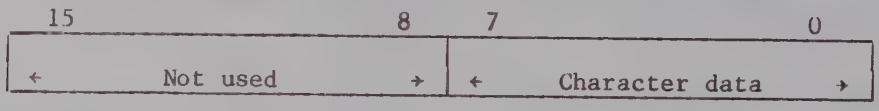
## Status registers

19. The formats of the control and status register (CSR) and the data buffer register (DBR) are shown below :-

i) CSR Address - 177514




ii) DBR Address - 177516




## TIMER/TERMINATOR BOARD AA7/1

Circuit diagram : Chap. 7, Figs. 9 & 10

### Introduction

20. The purpose of this board is to allow the use of DEC's multi-user operating system RSX-11M as an alternative to the single user operating system RT-11. The board performs the following functions :-

a) LSI-11 bus terminator
b) Programmable interval timer
c) Watchdog timer
d) Protection register
e) Line time clock control

These functions are all separate and independent of each other and are each described in turn below.

### LSI-11 bus terminator

21. 120 Ω terminations are provided for 22 address lines, of which 18 are at present implemented.

### Programmable interval timer

#### Operation

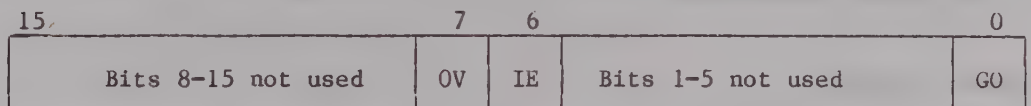
22. The timer consists of a 16-bit presettable counter driven from a crystal oscillator to provide the required interval. Output from 1 MHz crystal oscillator X1 is divided by IC31 and the resulting 10 kHz square wave is used to clock the up counter. This is formed by ICs 9,10,13 and 14. When LOAD COUNTER is asserted low from protocol logic IC4 via gate IC15, the counter is preset in 2's complement form to the required delay. When the signal is removed, the counter counts up until an overflow occurs which causes CARRY

from IC13 pin 12 to be asserted low. To pin 1 IC23, it clears the IC removing GO which halts the operation of the IC31 dividers. To pin 10 IC23, it presets the IC taking pin 9 high to assert BIT 7. This is taken to the CSR and is also ANDed by IC20 with IE from IC24 to assert RQSTA. When this occurs, interrupt logic IC3 requests a processor interrupt on the BIRQ 4 line at the lowest priority level. Tristate buffers IC18 and IC19 form a 16-bit register.

**Status registers**

23. The formats of the control and status register (CSR) and the data buffer register (DBR) are shown below :-

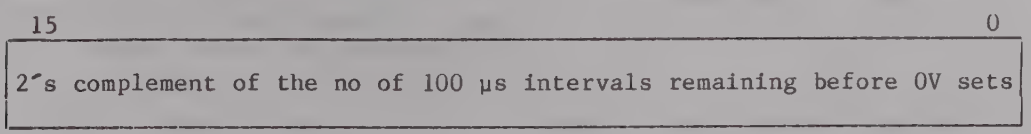
i) CSR Address - 177540




Bit definitions are as follows :-

| Bit | Description | | Function |
|---|---|---|---|
| 0 | GO | Read/write | Set by writing ´1´. Cleared by writing ´0´, by a BUS INIT signal on the Q-bus, or by the counter overflowing. When set, the counter is allowed to run and continually counts up. When clear, the counter is held (i.e. not clocked). |
| 6 | IE | Read/write | Set by writing ´1´. Cleared by writing ´0´, or by a BUS INIT signal on the Q-bus. When either OV or IE is set with the other signal already true, an interrupt is generated. |
| 7 | OV | Read only | Set by the counter overflowing. Cleared by writing ´1´ to GO or by a BUS INIT signal on the Q-bus. Causes an interrupt with IE when either one goes true with the other already true. |

ii) DBR Address - 177542




Prior to setting the GO bit in the CSR, the 2´s complement of the number of 100 µs periods required before an interrupt is generated is loaded into the DBR. GO is then set and the counter counts up to 0. The OV bit is then set, initiating an interrupt. The GO is also cleared when OV sets. Note that the DBR represents the contents of the counter registers at all times to enable the use of quick diagnostic testing and for the correct operation of the software handler.

## Watchdog timer

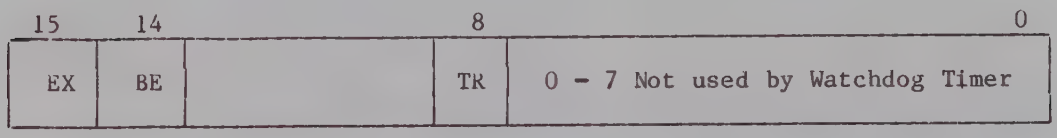
### Operation

24. This timer is used to automatically reboot the system in the event of a hardware or software malfunction. It consists basically of two retriggerable monostables IC28a and IC28b operating in series. Under normal operating conditions, IC28a is kept in its triggered state by clock pulses occurring at intervals of less than 50 ms. These clock pulses are provided either by TRIGGER from pin 11 IC15 (software generated) or from the SRUN line (hardware generated). Should the clock pulses fail to appear for more than 50 ms i.e. when a hardware or software crash has occurred, IC28a Q output goes low triggering IC28b which, via transceiver IC8, pulls down the BDCOK line for 2.2 µs. This forces the processor to execute its power fail restart sequence and so reboot the system.

### Status register

25. This device uses the high, unused byte of the programmable interval timer's CSR in the format shown below :-

CSR Address - 177542




| Bit | Description | | Function |
|---|---|---|---|
| 8 | TR | Write only | Set by writing '1'. Re-triggers the monostable to prevent the EX bit setting for a further period. |
| 14 | BE | Read/write | Set by writing '1'. Cleared by writing '0' or by BUS INIT on the Q-bus. If set, enables the watchdog timer to re-boot the system if the monostable enters the passive state. |
| 15 | EX | Read only | Set when the monostable is in the passive state. Cleared when the monostable is in the triggered or active state. |

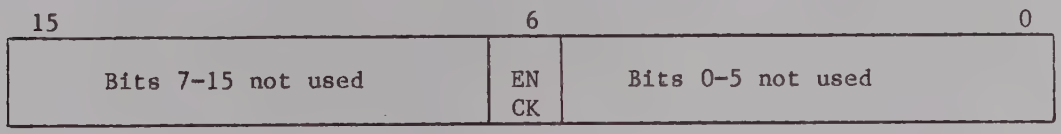
## Protection register

26. ICs 25 and 26 form a read-only register which holds a hard wired 16-bit binary sequence. This is for software protection to check that the board is only used in a compatible system. The CSR address is 177544.

## Line time clock control

27. ICs 29 and 30 form a second 16-bit CSR whose bit 6 provides a software means of enabling or disabling the line time clock. When bit 6 is reset, IC24b causes TR1 to switch on so earthing the BEVNT line to disable the 50 Hz clock. The register is read/write addressable :-

CSR Address - 177546



33. Unless certain memory locations are altered before running the program, a DLV11-J board must be patched to the addresses and vectors shown in Table 1.

TABLE 1 DLV11-J CHANNEL ADDRESSES

| Channel number | Base address | Base vector |
|---|---|---|
| 0 | 176500 | 300 |
| 1 | 176510 | 310 |
| 2 | 176520 | 320 |
| 3 | 177560 | 60 |

34. In addition to the Software Switch Register (SWR) there is another register, USWR (location 1220) that enables boards with other than standard patching to be tested. The user-selectable switch options are shown in Fig. 4.

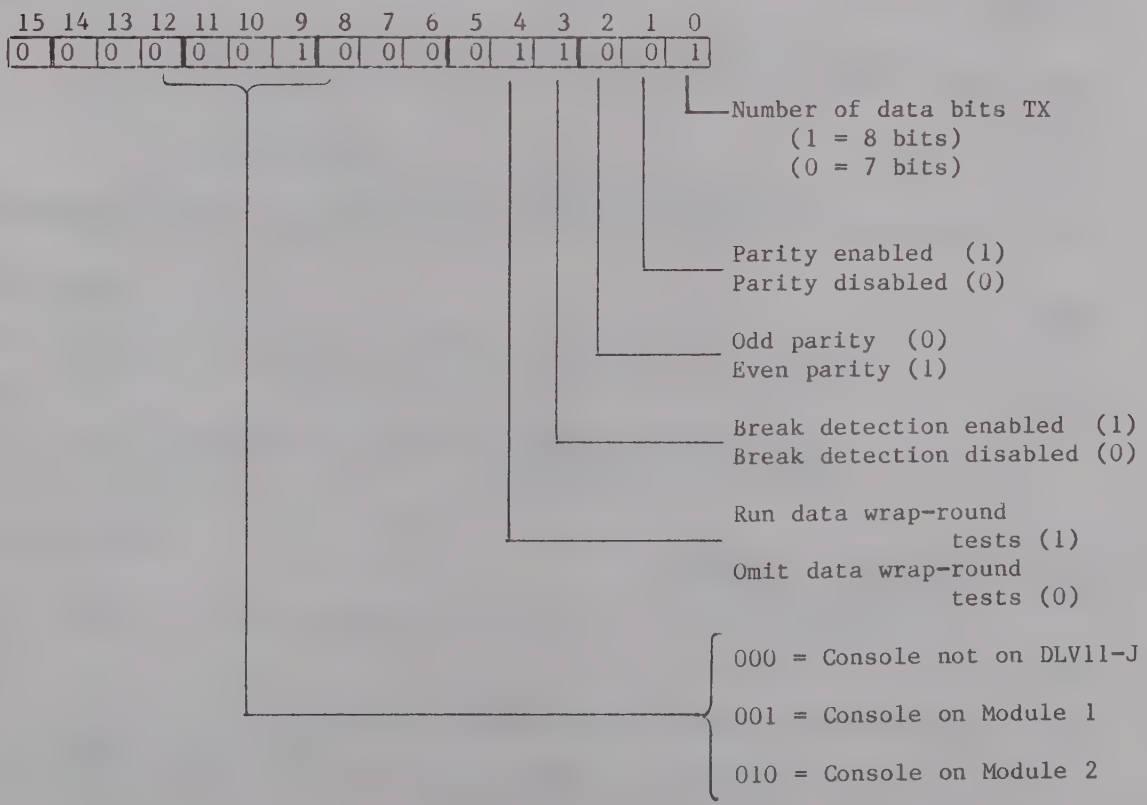

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 1 0 0 0 0 1 1 0 0 1
Number of data bits TX
(1 = 8 bits)
(0 = 7 bits)
Parity enabled (1)
Parity disabled (0)
Odd parity (0)
Even parity (1)
Break detection enabled (1)
Break detection disabled (0)
Run data wrap-round tests (1)
Omit data wrap-round tests (0)
000 = Console not on DLV11-J
001 = Console on Module 1
010 = Console on Module 2

Fig. 4 DLV11-J USWR user-selectable switch options

## Formatting floppy disks

31. The other function performed is the formatting of floppy disks. Normally disks are supplied with the correct format already recorded on them but this may be corrupted by exposure to stray magnetic fields etc. The format pattern also can deteriorate with use. A symptom of this is the increasing difficulty with which data is read from the disk in question (note that there are other possibilities here). Using this second function some disks may be restored to health. Note, however, any recorded information will be destroyed by the formatting process and thus should, if possible, be copied to another storage volume.

| | |
|---|---|
| .R D440?? | Run D440 test |
| REMOVE DIAGNOSTIC DISKETTE | Remove XXDP disk |
| DSD FLOPPY DISK DIAGNOSTIC WITH FORMAT CAPABILITY<br>TYPE 'A' TO DO ACCEPTANCE TEST ON 2 DRIVES<br>ON DEVICE 177170 (10 MIN) | |
| TYPE 'X' TO FORMAT A DISKETTE. PROGRAM WILL ASK UNIT#.<br>TYPE 0, 1 OR 2. PROGRAM WILL ASK SEQ FORMAT:?<br>TYPE Y FOR STANDARD, N FOR INTERLEAVED FORMAT. | |
| DSD FRDTST V5B<br>(0-167776) | |
| #MODE:XFORMAT REALLY?Y | Type "X" then "Y" |
| UNIT:<0 or 1> | Select drive followed by carriage return |
| SEQUENTIAL FORMAT?Y | Just type "Y" |
| DENSITY (S)INGLE OR (D)EC-DOUBLE:S or D | Select appropriate density formatting commences. |
| #MODE: | Test ready for commands. |

Note ...

Sequential format should be specified when creating disks for use on Marconi Instruments Ltd. equipment.

## ▶ DLV11-J DIAGNOSTIC - VDLABO.BIC

32. This diagnostic is a logic test to verify the operation of the DLV11-J serial interface. Testing is done in two phases:

(1) All selected channels are tested individually.

(2) The DLV11-J module is tested as a whole for channel interaction problems. This diagnostic is designed to test and detect errors to the logic level.

29. The Short test takes approximately ten minutes for one pass while the full Acceptance test may take anything up to an hour to complete.

30. All test modes produce a fair amount of console output, even when no faults are found, but all error reporting text is self evident as shown below.

Note ...

Don't forget to remove the copy of XXDP and insert two good scratch-disks for use by the Read/Write test. (Write enabled disks please.)

Short test

```
#DD MODE:SHORT SCAN CRC CHECKED WRITING READING INTERRUPT ENABLED
     WRITING READING FILL-EMPTY RANDOM-RD/WRT READING DEN = 0
PASS FIN

         UN0  #BAD=0 #RD/WRT=1707  #XFERS=10161  B-DATA=0
         UN1  #BAD=0 #RD/WRT=1716  #XFERS=1532   B-DATA=0

     SCAN .........
```

Acceptance test

```
#DD MODE:ACCEPTANCE TEST SCAN CRC CHECKED WRITING READING INTERRUPT
     ENABLED WRITING READING FILL-EMPTY RANDOM-RW READING DEN=0
PASS FIN

         UN0  #BAD=0  #RD/WRT=20526  #XFERS=53607  B-DATA=0
         UN1  #BAD=0  #RD/WRT=19101  #XFERS=14864  B-DATA=0
*^2^3^4^5^6^7^10^11^12^13^14^15^16^17^20^21^22^23^24^25^26^27 **...
```

Verify test

```
#DD MODE:VERIFY TEST SCAN CRC CHECKED WRITING READING INTERRUPT
     ENABLED WRITING READING FILL-EMPTY RANDOM-RD/WRT READING DENS=0
PASS FIN
         UN0=0  #BAD=0  #RD/WRT=1707  #XFERS=10161  B-DATA=0
         UN1=1  #BAD=0  #RD/WRT=1716  #XFERS=1532   B-DATA=0
*SCAN CRC CHECKED

PROCEEDING SCAN                          | Starts full Acceptance Test
                                         | here but without normal
                                         | printout except errors
```

Note ...

Tests can be stopped at any time by typing <control>R to return to the "MODE:" prompt level.

(i) A check for correct printout of single and double width characters.

(j) A check for correct operation when printing under interrupt control from the processor.

(k) A check is made on the programmed select and deselect commands.

If all the foregoing are satisfactory 'END OF TEST' is printed and the program halts in ODT and displays the "@" sign on the VDU.

26. To re-run the program or restart after an error condition type 1000G. Any time an error condition is encountered the program will halt in ODT and display an "@".

## D44000 DIAGNOSTIC FOR DSD 440 FLOPPY DISK DRIVE

27. The diagnostic package supplied for checking the DSD 440 floppy disk system originates from Data Systems Design. This provides several features in addition to the testing capability including disk formatting and copying. Details of these ancillary functions can be found in the DSD 440 manual supplied with the disk drive sub-assembly. The DSD 440 package is run from the XXDP system disk by the "R" command as normal and will introduce itself as follows :-

```
.R D440??                                    | Run D440 test from
                                             |       XXDP
REMOVE DIAGNOSTIC DISKETTE                   | Remove XXDP disk if
                                             | XXDP is resident on
DSD FLOPPY DISK DIAGNOSTIC WITH FORMAT CAPABILITY |     floppy
TYPE 'A' TO DO ACCEPTANCE TEST ON 2 DRIVES
ON DEVICE 177170 (10 MIN)

TYPE 'X' TO FORMAT A DISKETTE.  PROGRAM WILL ASK UNIT#.
    TYPE 0, 1 OR 2.  PROGRAM WILL ASK SEQ FORMAT:?
    TYPE Y FOR STANDARD, N FOR INTERLEAVED FORMAT.

DSD FRDTST V5B
(0-167776)                                   | Memory size in bytes

#MODE:
```

At this point the appropriate command to perform the required function must be entered. "A" for Acceptance test, "SH" for SHort test, "X" for disk formatting and "DUP" for disk copying. Other commands do exist but are not described here. Details can be found in the DSD manual.

## DSD 440 diagnostic tests

28. The basic diagnostic can be run in one of three modes, Short, Acceptance and Verify. The Short mode limits all tests to just the first eight tracks on the diskette thus allowing a complete test scan of all functions to be completed in a relatively short time. Acceptance mode performs the testing procedure over all tracks, this is more thorough and thus may identify less common or intermittent faults that the Short test might miss. Finally, Verify mode can be specified to combine the advantages of the Short and Acceptance tests. First a Short test is performed for one pass in order to find fundamental faults quickly and then the test limits are expanded to those of the full Acceptance test which is then run.

Remote functions

22. Fully testing this facility requires the use of a special jig which is not normally available for customer servicing. Omit this section by pushing any key on the keypad. The display will show 'END OF TESTS' and, after a pause, the program will restart.

## CENTRONICS 780/781 PRINTERS DIAGNOSTIC - LPRTXX

23. Digital Equipment Corp., have written a very comprehensive diagnostic routine for their LA180 printers. This routine DZLA?? has been adapted here for testing Centronics 7800/781 printers.

24. There are several minor differences electrically between an LA180 with its interface and a 780 or 781 with an AM12 interface. The relevant sections of DZLA have been adapted in LPRT to take account of these differences. In addition all sections of DZLA involving use of the keyboard have been ignored. Introducing LPRT, and extra facilities such as alternative address and vector patching, loop on test etc., have been omitted from LPRT. However LPRT contains additional routines to test facilities on a 780 or 781 which are not available with an LA180 such as double width character printing etc.

Program details

25. The following tests outlined below are carried out in the order shown :-

(a) 16 full lines of alternate '*' and 'U' are printed to test the seven data lines. The ASCII codes for these characters are complementary.

(b) A single line of alternate '0' 'space' is printed. The spaces are then filled one at a time by an 'X' to test the head positioning for single characters.

(c) A printout of the whole printable character set, lines of 24 characters, are printed sequentially in ascending ASCII order.

(d) A test for malfunction when non-printable (control) characters are fed to the printer. Non-printable characters are loaded into the printer buffer before and after a section of 80 printable characters and then a line is printed. The result should be a 30 full line printout in the form of a single step swirl pattern of printable characters.

(e) Correct operation of the character buffer is tested by filling it with 'E' (for error) characters and then replacing the 'E' characters by first 'I' characters and then space characters. Any 'E' printout is a fault. This is followed by a print of the number of each of the 80 columns from 01 to 80 to check the column count.

(f) Overprint accuracy is checked by 4 consecutive lines of double over-printing. The 4 lines are filled with character pairs 'E' 'space'; 'space' '@'; 'M' 'space'; 'space' '#' respectively.

(g) Multiple line feed is checked by successively actuating 1,2,4,8,16 and 32 line feeds.

(h) Bell test is included in case this option is supplied. The audible alarm should sound five times.

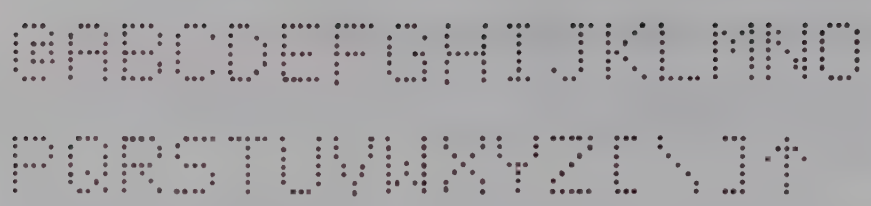



Fig. 1 TK 1803 Alphanumeric Display - First set of characters test.

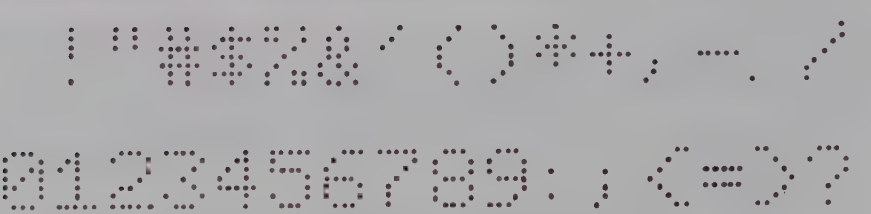



Fig. 2 TK 1803 Alphanumeric Display - Second set of characters test.

Fig. 3 TK 1803 Alphanumeric Display - Line addressing test.

17. This section of the program starts with a delay of several seconds for the operator to transfer his view from the v.d.u. to the display. The characters are written singly at roughly half second intervals from left to right first filling the top row and then the bottom row. The display should then appear as in Fig. 1. After a delay of several seconds the display is then progressively overwritten in the same order by a second set of characters, finally appearing as in Fig. 2. After a further delay of several seconds the programmable backspace facility is tested by completely overwriting the display in reverse order by a set of asterisks. Another delay of several seconds is followed by a high speed blanking operation which successively overwrites each asterisk with a blank space at maximum system speed. Finally after another delay of several seconds the caption in Fig. 3 is written on the display at high speed, lower line first, to test for correct line addressing.

## Output functions

### Keypad

18. In this section the operator is required to push each keypad button in turn. The number of the button pushed is then displayed on the alphanumeric display. Buttons may be pushed in any order. When the program has recognized that each button has been pushed at least once it will proceed to the next section. Pushing a keypad button within about 100 ms of the previous button, or before the previous button has been released, will not be registered. Operating controls other than keypad buttons in this section will result in the program restarting the section.

### Control buttons

19. In this section the operator is required to push each button in turn. As he does so the number of the button he pushes is displayed on the alphanumeric display. Buttons may be pushed in any order. The grey button is tested within this section as follows :-

(i) Push the grey button and note that its lamp lights

(ii) Hold the grey button depressed and press any other control button and note that its number is displayed

20. When the program recognizes that each control button has been pressed at least once it will proceed to the next section. Pressing a control button within about 100 ms of the previous button, or before the previous button has been released will not be registered. Operating controls other than control buttons in this section will result in the program restarting the section.

### Secure/enable key

21. In this section the operator is required to turn the key once and then back again. Each time he turns the key the alphanumeric display shows the position to which the key has been turned. Operating controls other than the key in this section will result in the program restarting the section.

commands are used where some modification to a diagnostic is necessary, for instance if a basic test requires tailoring to the current hardware configuration. The test is loaded from disk and the microcode ODT commands are used to change its control parameters etc. Where no operator modification is required the "R" command may be used to load and execute a test without further intervention. XXDP commands available are as follows :

F<CR> TO SET CONSOLE FILL COUNT
D<CR> FOR DIRECTORY ON CONSOLE, OR
D/F<CR> FOR SHORT DIRECTORY ON CONSOLE, OR
D/L<CR> FOR DIRECTORY ON LINE PRINTER, OR
D/L/F<CR> FOR SHORT DIRECTORY ON LINE PRINTER
R FILENAME<CR> TO RUN ANY OTHER PROGRAM
L FILENAME<CR> TO LOAD A PROGRAM ONLY
S<CR> TO START THE PROGRAM JUST LOADED
S ADDR<CR> TO START THE PROGRAM AT SPECIFIC ADDRESS
C FILENAME<CR> TO RUN A CHAIN
C FILENAME/QV<CR> TO RUN A CHAIN IN QUICK VERIFY MODE

## CONTROL PANEL TK 1803 DIAGNOSTIC CPANXX

12. This program is essentially a sequential test routine to give assurance of the correct function of a TK 1803 Control Panel. In the event of a malfunction no diagnostic assistance is provided and the service engineer must decide for himself a suitable procedure for fault diagnosis to component level. The program is divided into three sections testing display functions, output functions and remote functions.

### Display functions

13. Each of the display functions is tested in turn with suitable program delays to enable an operator to easily spot a malfunction.

#### Annunciators

14. The annunciators are an array of 10 l.e.d. lamps arranged in 2 rows of 5. The program starts with a delay of several seconds to allow the operator to transfer his view from the v.d.u. screen to the annunciator array. The annunciators are then singly lit and extinguished at roughly half second intervals in the order top left to bottom right.

#### Button lamps

15. There are two groups of buttons, a group of 7 and a group of 5. Each button has an inbuilt amber l.e.d. lamp. A delay of several seconds allows the operator to transfer his view from the v.d.u. to these buttons. Each button lamp is then singly lit and extinguished at roughly half second intervals from left to right. There is a pause of several seconds between lighting lamps in the group of 7 and the group of 5. The lamp in the left-hand (grey) button of the group of 5 cannot be lit under program control and only lights when its button is pressed.

#### Alphanumeric display

16. The display has 32 character positions in two rows of 16. It is capable of displaying any 62 different characters (English font ROM, other fonts available) and a blank space in any of the 32 positions.

```
ENTER DATE (DD-MMM-YY) : <RETURN>

RESTART ADDR : 153726
LSI?   N   <RETURN>

THIS IS XXDP+   TYPE "H" OR "H/L" FOR DETAILS
```

9. Finally XXDP issues a full stop (".") as a prompt to indicate its readiness to accept commands. Note there is NO TYPE AHEAD in XXDP. At this point it may be useful to list the disk contents onto the system line printer if one exists. This is done as shown in the directory example below. This directory will be of use when attempting to run the most up-to-date versions of the various diagnostic programs.

## DISPLAYING CONTENTS OF XXDP DISK

10. Once the XXDP monitor has prompted for commands by "." the "D" or "D/F" commands may be entered to list the system disk directory on the console. Unfortunately, the directory tends to be longer than twenty four lines so that the first items are lost from view if no action is taken. The only way to stop this from happening is to press the BREAK key at a convenient point, read the start of the directory listed and then press P to proceed with the remainder. However, if the current controller system has a line printer (at the preferred address of 177514) the directory listing may be output there instead, by means of the "D/L" command, thus giving a hard copy for future reference.

Note ...

No check is made for the presence of the line printer and XXDP will crash if the preferred address does not respond.

Directory example

```
.D<cr>

ENTRY#  FILNAM.EXT        DATE        LENGTH START

000001  RXDP  .BIN      16-JAN-80       17   000050
000002  UPD2  .BIN      16-JAN-80       29   000071
000003  ZRXAE0.BIC      16-JAN-80       20   000126
000004  ZRXBE0.BIC      16-JAN-80       17   000152
000005  VKAAC0.BIC      16-JAN-80       17   000173

        ...  ...  ...  ...  ...  ...  ...  ...
        ...  ...  ...  ...  ...  ...  ...  ...
        ...  ...  ...  ...  ...  ...  ...  ...

000031  CPAN05.BIN      16-JAN-80        5   000571
000032  MCLK01.BIN      16-JAN-80        9   000576
000033  181101.BIN      16-JAN-80        3   000607
```

## LOADING AND RUNNING XXDP DIAGNOSTICS

11. Individual diagnostics are loaded and run by means of three simple commands. "L" for Load, "S" for Start and "R" for automatic load and start combined. The actual command to be used depends upon the test in question and is shown under the diagnostic headings. Normally the "L" and "S"

diagnostic software, i.e. if the system exhibits a major fault it may be impossible to use XXDP to find it. If this should be the case, the only course of action is to contact the Service Dept. The minimum working configuration is itemized below. Note that if the symptoms are intermittent it may be possible to run XXDP even if the fault is with one of the sub-systems below :-

(i) A central processor capable of executing its "Basic" instruction set.

(ii) 8 K of working memory with addresses 0 - 40000 octal.

(iii) An operational serial line interface for the console. XXDP does not operate this interface under interrupts so a fault is acceptable here.

(iv) An operational disk system capable of reading the XXDP volume. Again XXDP does not use interrupts for this operation. Note, however, that some peripherals use DMA to transfer data so this function must be fully operational for these devices.

## GETTING STARTED WITH XXDP

6. Marconi Instruments supply two copies of XXDP as part of the standard software set. These should be considered to be masters and preserved accordingly. A copy should have been made for active use using the RT-11 program "DUP". If no copy is available one should be made before proceeding. However if this is impossible due to hardware failure one of the supplied copies may be used out of necessity. Extreme care should be taken to ensure that no data corruption occurs.

Note ...

Should a master copy be accidentally destroyed on no account use the other master in the same circumstance as this could be corrupted also. The master archive must be made up to two copies as soon as possible.

7. Before trying to run XXDP check that the +5 V OK, +12 V OK, AC OK and RUN lamps are On in the controller PSU. Check also that the front panel ENABLE/DISABLE key switch is set to the ENABLE position. The line time clock should be turned off by means of the switch at the back of the controller. Then the active copy of XXDP should be placed in drive 0 of the appropriate peripheral and the controller "booted". This may be done by applying mains power to the complete hardware system. If XXDP fails to boot check for any obvious loose connections. If this still fails to clear the fault contact Marconi Autotest Service Department.

8. Once the executive software of XXDP has been loaded from the disk it will start automatically and announce its presence, type and version number. XXDP then lists the simple commands available for listing the contents of the disk, loading and running the diagnostic programs as in the following example :-

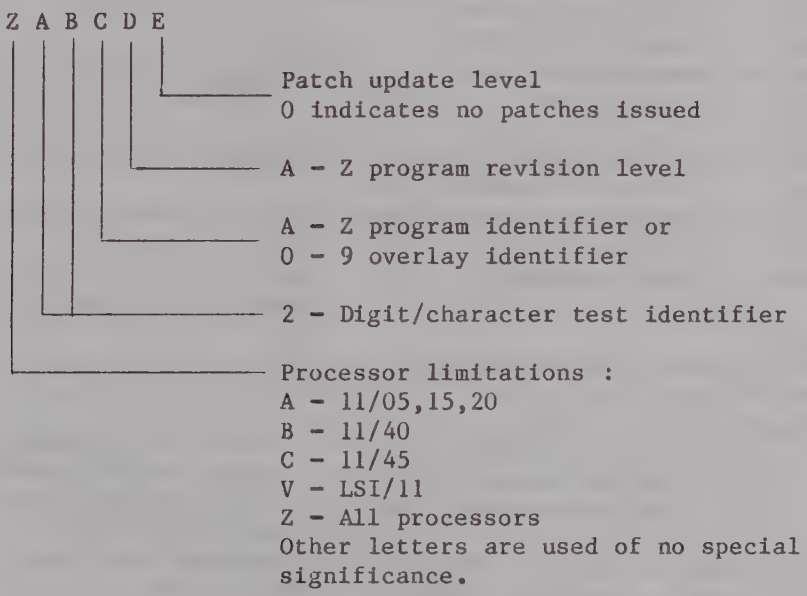
```
Auto-Boot OR @173020G

CLEARING MEMORY
CHMDYAO XXDP+ DY MONITOR 28K
BOOTED VIA UNIT 0
```

the peripheral in which it resides, e.g., the XXDP monitor produced to reside and run from an RX01 floppy disk drive is called "RXDP". The XXDP monitor provides the means of loading and starting the individual test programs. It also allows the listing of the system medium thus enabling a particular test program to be located. The diagnostic programs are identified by a filespec consisting of six unique characters derived from the test option name combined with the revision or update code and a three character extension indicating the file format. These complete names are used to instruct the monitor to load and execute each test program as required.

## FILE NAME CONVENTIONS

4. The test program file names are constructed using the following convention :-

Filespecs


Z A B C D E
Patch update level
0 indicates no patches issued
A - Z program revision level
A - Z program identifier or
0 - 9 overlay identifier
2 - Digit/character test identifier
Processor limitations :
A - 11/05,15,20
B - 11/40
C - 11/45
V - LSI/11
Z - All processors
Other letters are used of no special
significance.

Extensions

| | |
|---|---|
| .BIN | Program in ABS format (in blocks with checksum) |
| .SAV | Program stored as direct memory image |
| .BIC | Program in ABS format but is chainable |

Note ...

Sections D and E of the file name may be replaced by two "?" marks when loading or running the diagnostics. The XXDP monitor then automatically locates the first test, on the disk, of that name irrespective of the version or patch levels. It is stressed that this method of referencing files will locate the first sequential file of the correct name and not necessarily the highest version/patch revision.

e.g. VKAA?? will find VKAA01 etc.

## OPERATIONAL LIMITATIONS OF XXDP

5. Once loaded, XXDP and its collection of test programs is capable of finding and localizing the majority of TK 1802 Controller faults. However, the system must be operating after a fashion in order to load and execute the

# Chapter 5

## MAINTENANCE

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## GENERAL

1. Various self-test and diagnostic programs for items associated with the TK 1802 Series Controllers are available on a floppy disk. The title of the disk can be RXDP or RYDP depending upon whether the recording technique used is single density or double density format respectively,

2. This chapter is intended as an aid in using the diagnostic software and provides a brief description of the system monitor, XXDP and all the supplied test programs. The descriptive text, while not comprehensive, is intended to be sufficient to enable faults to be determined down to sub-system or board level but not necessarily to specify the exact fault.

## INTRODUCTION

3. XXDP is the general name given to a comprehensive family of diagnostic programs. These consist of the monitor, XXDP itself, and various test programs which enable the source of any system malfunction to be located. The actual name of the monitor differs from system to system depending upon

35. The default value of USWR is 1031, i.e.

8 bits transmitted
Parity disabled
Odd parity
Break detection enabled
Run data wrap-round tests
Console on Module 1

These functions match those of a board with standard patching in accordance with Fig. 9 in Chap. 3. Should it be necessary to change any function refer to step (j) under 'Test procedure' given below.

**Test procedure**

36. Proceed as follows:-

(a) Ensure that the DLV11-J board has jumpers connected as shown in Fig. 9 in Chap. 3.

(b) Ensure that the mains power to the mainframe unit is turned OFF.

(c) Insert XXDP disk 59000-031 into drive 0 of the disk unit.

(d) Fit wrap-round links to channels 0, 1 and 2 of the board to be tested (these channels are labelled J0, J1 and J2).

(e) Disconnect the v.d.u cable from channel 3 (J3) of the DLV11-J board in the mainframe unit. Unplug this board and replace it with the board to be tested. Connect the v.d.u. cable to channel 3.

(f) Turn On the power to the mainframe unit.

(g) If channel 3 of the DLV11-J board is functioning the v.d.u. will show the following:

| VDU | Operator |
|---|---|
| CLEARING MEMORY | |
| CHMDYAO XXDP + DYMONITOR 28 K | |
| BOOTED VIA UNIT 0 | |
| ENTER DATE (DD-MM-YY): | <RETURN> |
| Restart ADDR: 153726 | |
| LSI ? N | <RETURN> |
| This is XXDP + TYPE "H" or "H/L" for details | <RETURN> |

(h) If the v.d.u. displays nothing or random characters or there is no response when RETURN is pressed :

i) The DLV11-J board is faulty or,

ii) The DLV11-J console (channel 3) address or vector jumpers have been set incorrectly or,

iii) The DLV11-J channel 3 communication parameters have been set incorrectly or do not match those of the VT 100 terminal.

These parameters should be:

9600 baud
Odd parity
8 data bits
1 stop bit
Parity inhibited

To check the v.d.u. parameters:

Press SET UP
Press 5

This will cause SET-UP to be displayed (see Fig. 5)
The parameters in block 4 should match those shown in Fig. 5.

To change a parameter, position the cursor over the parameter to be changed and press 6.

To EXIT, press SET UP.

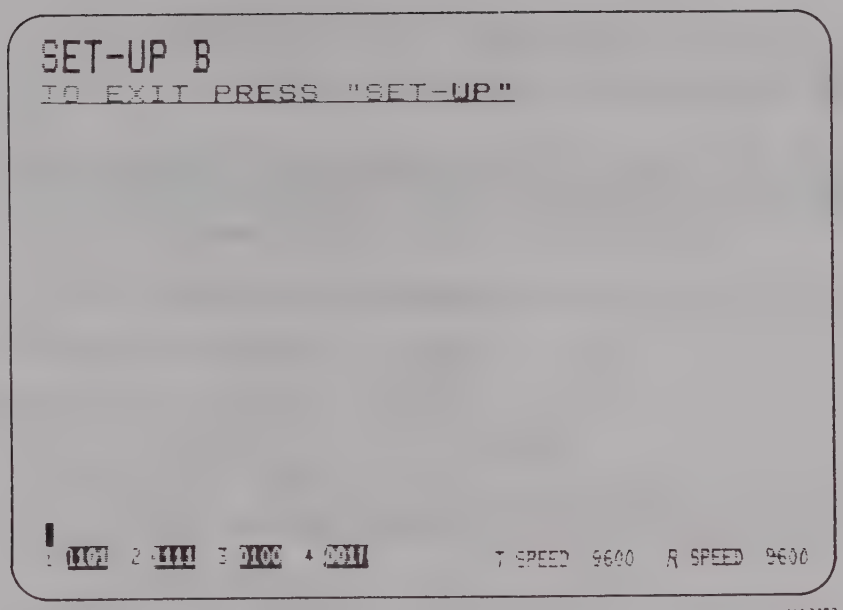
(Note that the test program does not care what the console communication parameters are, provided they match those patched on the DLV11-J board).

(i) If the v.d.u. displays meaningful messages and responds to keyboard inputs, enter:

LOAD VDLABO.BIC <RETURN>

(j) If the board under test has standard patching proceed to (k) below; if it is necessary to modify the contents of VSWR (location 1220) use the procedure as in the following example which causes the data wrap-round tests to be omitted:-

| VDU | Operator |
|---|---|
| | <BREAK> |
| @ | 1220/ |
| @ 1220/1031 | 1011 <RETURN> |
| @ 1220/1031 1011 | |
| @ | 153726G |
| @ 153726G | |



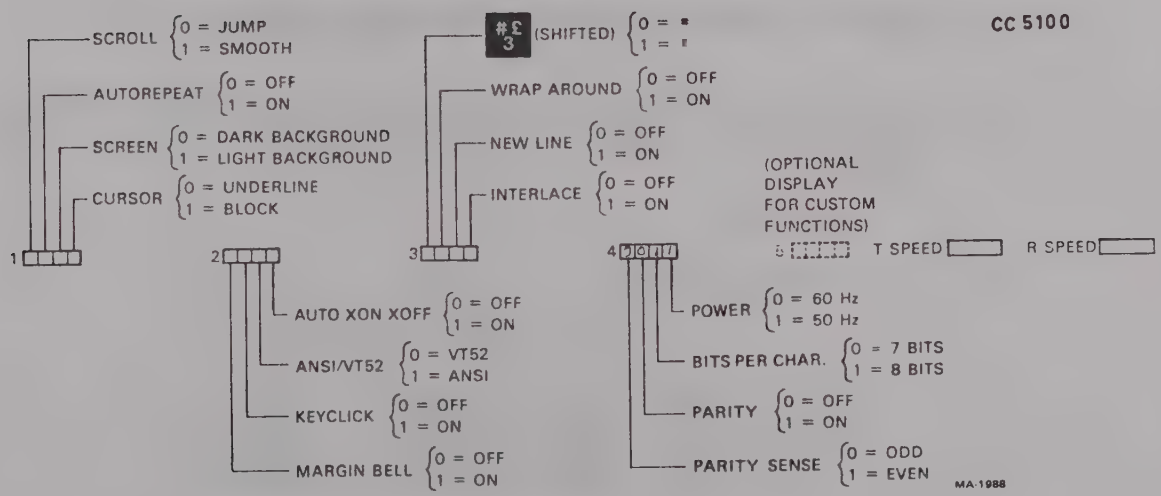


CC 5100
SCROLL 0 = JUMP 1 = SMOOTH
AUTOREPEAT 0 = OFF 1 = ON
SCREEN 0 = DARK BACKGROUND 1 = LIGHT BACKGROUND
CURSOR 0 = UNDERLINE 1 = BLOCK
#£ 3 (SHIFTED) 0 = # 1 = £
WRAP AROUND 0 = OFF 1 = ON
NEW LINE 0 = OFF 1 = ON
INTERLACE 0 = OFF 1 = ON
(OPTIONAL DISPLAY FOR CUSTOM FUNCTIONS)
5 T SPEED R SPEED
AUTO XON XOFF 0 = OFF 1 = ON
ANSI/VT52 0 = VT52 1 = ANSI
KEYCLICK 0 = OFF 1 = ON
MARGIN BELL 0 = OFF 1 = ON
POWER 0 = 60 Hz 1 = 50 Hz
BITS PER CHAR. 0 = 7 BITS 1 = 8 BITS
PARITY 0 = OFF 1 = ON
PARITY SENSE 0 = ODD 1 = EVEN
MA-1988

Fig. 5 DLV11-J Mode B presentation and summary.

(k) Enter the following (but see Fig. 6 for the software switch register options):-

| VDU | Operator |
|---|---|
| | S200 <RETURN> |
| CVDLxx 0 DLV11-J Test | |
| SWR = 000000 NEW | 16000 <RETURN> |

The test program will now start.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | |
|---|---|---|---|
| Bit 15 set | = | 100000 | = HALT on Error |
| 14 | = | 40000 | = Loop on Test |
| 13 | = | 20000 | = Inhibit error messages |
| 12 | = | 10000 | = Enable performance reports |
| 11 | = | 4000 | = Inhibit Iterations |
| 10 | = | 2000 | = Bell on Error |
| 9 | = | 1000 | = Loop on Error |
| 8 | = | 400 | = Loop on Test in 7 to 0 |
| 7 to 0 | = | 0 - 377 | = No. of Test to LOOP on |

Fig. 6 DLV11-J software switch register options

(l) An example of the display for a board with no faults is shown in Fig. 7 (Note: Ignore any random characters that may also appear).

```
WILL TEST

MODULE 1 CHANNEL  0  1  2  3

                    *** PHASE 1 SUMMARY ***

CSR: 176500,    VECTOR:  000300,    ERRORS:  0
CSR: 176510,    VECTOR:  000310,    ERRORS:  0
CSR: 176520,    VECTOR:  000320,    ERRORS:  0
CSR: 177560,    VECTOR:  000060,    ERRORS:  0

                    *** PHASE 2 SUMMARY ***

CSR: 177560     VECTOR:  000300,    ERRORS:  0

END PASS # 1
```

Fig. 7 DLV11-J example of the display for a board with no errors

(m) The program will now loop until either:

i) BREAK is pressed - this will cause the processor to enter console ODT microcode.

ii) CTRL G is pressed - this will cause the program to ask for a new SWR word.

It will be necessary to press these keys several times as the program only scans the keyboard infrequently and sends out RESET signals frequently - it is advisable to hold the key down until the program stops.

Should the v.d.u. ´KBD LOCKED´ l.e.d. come on, or the program does not respond when BREAK or CTRL G is pressed, press SET UP then ´RESET´ 0 to reset the v.d.u.

To restart the test program after entering console ODT microcode enter:

153726G

then S200 <RETURN>

(n) If the board under test shows no errors after approx. 10 passes of the program, turn OFF the power to the mainframe unit and remove the board.

(o) Should the board have a fault the v.d.u. will display an error message in the format:

TEST ...., ERROR ..... PC.....ADDRESS.....VECTOR.....

Where ADDRESS and VECTOR refer to the failing DLV11-J channel and all values are in octal.

# Chapter 6

## REPLACEABLE PARTS

CONTENTS

Para.
1 Introduction
3 Abbreviations
4 Component values
6 Ordering
7 Components
7 Unit A0 - Main frame
8 Unit A1 - Switch panel
9 Board AA7/1 - Timer/terminator
10 Board AM12 - Printer interface
11 Mechanical parts
Accessories - see Chap. 1

## INTRODUCTION

1. Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification, e.g. A0, AA7 etc.

2. The complete component reference carries its unit number as a prefix e.g. AM12C3 (capacitor C3 on the AM12 board) but for convenience in the text and on circuit diagrams the prefix is not used. However, when ordering replacements or in correspondence the complete component reference must be quoted.

## ABBREVIATIONS

3. The components are listed in alphanumerical order of the complete circuit reference and the following abbreviations are used :-

| | | | | | |
|---|---|---|---|---|---|
| C | : | capacitor | R | : | resistor |
| Carb | : | carbon | S | : | switch |
| Cer | : | ceramic | SK | : | socket |
| D | : | semiconductor diode | T | : | transformer |
| Elec | : | electrolytic | Tant | : | tantalum |
| FS | : | fuse | TP | : | test point |
| IC | : | integrated circuit (package) | TR | : | transistor |
| L | : | inductor | Var | : | variable |
| LK | : | link | W | : | watts at $70^0$ C |
| Met | : | metal | X | : | ferrite bead |
| PL | : | plug | † | : | values selected during test; nominal value listed. |
| Plas | : | plastic | | | |

## COMPONENT VALUES

4. One or more of the components fitted in this instrument may differ from those listed in this chapter for any of the following reasons :-

a) Components indicated by a † have their values selected during test to achieve particular performance limits.

b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the instrument is maintained.

c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the instrument.

## ORDERING

6. When ordering replacements address the order to our Service Division (address inside rear cover) or nearest agent and specify the following for each component required :

(1) Type* and serial number of instrument

(2) Complete circuit reference

(3) Description

(4) Marconi Instruments code number

*As given on the serial number label at the rear of the instrument; if this is superseded by a model number label, quote the model number instead of the type number.

COMPONENTS

## 7. Unit A0 - Main frame

When ordering, prefix circuit reference with A0.

| Circuit reference | Description | Code No. |
|---|---|---|
| | Power supply unit | 46662-073H |
| | LTC cable, 3-way, with toggle-switch SA | 43129-493K |
| | DC power cable, 9-way | 43130-005M |
| | LSI-11 signals cable, 12-way | 43130-006C |
| FS1,FS2 | OUTLET, 5A, quick acting | 23411-009J |
| FS3 | 12V OUTLET, 500mA, delay | 23411-056X |
| | Fuseholder (1 of 3) | 23416-192R |
| | Fuseholder cover (1 of 2) | 23416-198E |
| FS4,FS5 | Thermal fuse assembly, 77$^0$C | 43289-002H |
| PLA | SUPPLY IN, 3-pin | 23423-150L |
| | Protective cover | 37590-150P |
| PLB | DUNNO, 3-pin | 23423-156W |
| RLA | Relay | 23486-154Z |
| SKC | To switch panel assembly/TK 1803, 3-way | 23423-160Z |
| SKD | SUPPLY OUT, 3-way | 23424-161H |
| SKE | 12V OUTLET, 3-way | 23427-124L |
| SKF | Receptacle | 23435-512X |
| | Pin (1 of 2) | 23435-590H |
| | Socket | 23435-591E |
| SKH | Receptacle | 23435-178U |
| | Housing, 3-way | 23435-171R |

## 8. Unit A1 - Switch panel

When ordering, prefix circuit reference with A1

| | | |
|---|---|---|
| | 12 V supply cable, with 5-way socket | 43129-217R |
| FS1,FS2 | Fuse 1A (230V), super delay | 23411-066Z |
| | Fuse 2A (115V), super delay | 23411-067H |
| | Fuse holder (1 of 2) | 23416-192R |
| | Fuse holder cover (1 of 2) | 23416-198E |
| PLM | 230V supply in | 23423-159P |
| | Cover | 23423-999Y |
| SA | Push-button | 23465-297M |
| | Lamp 12V | 23735-456E |
| SB | Key-operated | 23462-056F |
| SKM | 230V supply out | 23424-161H |

## 9. Board AA7/1 - Timer/terminator

When ordering, prefix circuit reference with AA7

| Circuit reference | Description | Code No. |
|---|---|---|
| | Complete assembly | 44828-778B |
| C1 | Elec 22µF 20% 25V | 26421-114E |
| C2 | Elec 22µF 20% 25V | 26421-114E |
| C3 | Plas 470pF 2% 63V | 26538-635X |
| C4-27 | Cer 10nF 20% 50V | 26346-120Y |
| C28 | Plas 470pF 2% 63V | 26538-635X |
| C29-33 | Cer 10nF 20% 50V | 26346-120Y |
| C34 | Tant 2.2µF 20% 20V | 26486-540K |
| C35-38 | Cer 10nF 20% 50V | 26346-120Y |
| IC1 | DC005 | 28469-405H |
| IC2 | DC005 | 28469-405H |
| IC3 | DC003 | 28469-403A |
| IC4 | DC004 | 28469-404Z |
| IC5 | DC005 | 28469-405H |
| IC6 | DC005 | 28469-405H |
| IC7 | 74LS04 | 28469-171L |
| IC8 | N8T38B | 28469-175V |
| IC9 | 74LS193 | 28464-126C |
| IC10 | 74LS193 | 28464-126C |
| IC11 | 74LS00 | 28466-345H |
| IC12 | 74LS04 | 28469-171L |
| IC13 | 74LS193 | 28464-126C |
| IC14 | 74LS193 | 28464-126C |
| IC15 | 74LS00 | 28466-345H |
| IC16 | 74LS04 | 28469-171L |
| IC17 | 74LS00 | 28466-345H |
| IC18 | 74LS541 | 28469-195H |
| IC19 | 74LS541 | 28469-195H |
| IC20 | 74LS08 | 28466-012L |
| IC21 | 74LS373 | 28462-410E |
| IC22 | 74LS373 | 28462-410E |
| IC23 | 74LS74 | 28462-611A |
| IC24 | 74LS74 | 28462-611A |
| IC25 | 74LS541 | 28469-195H |
| IC26 | 74LS541 | 28469-195H |
| IC27 | 74LS74 | 28462-611A |
| IC28 | 74LS123 | 28468-309B |
| IC29 | 74LS541 | 28469-195H |
| IC30 | 74LS541 | 28469-195H |
| IC31 | 74LS390 | 28464-127R |

9. **Board AA7/1 - Timer/terminator** (continued)

| Circuit reference | Description | Code No. |
|---|---|---|
| R1 | Package 8x180/390Ω 2% | 24681-616C |
| R2 | Package 8x180/390Ω 2% | 24681-616C |
| R3 | Package 8x180/390Ω 2% | 24681-616C |
| R4 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R5 | Package 8x180/390Ω 2% | 24681-616C |
| R6 | Package 8x180/390Ω 2% | 24681-616C |
| R7 | Package 8x180/390Ω 2% | 24681-616C |
| R8 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R9 | Met film 2.2kΩ 2% 1/4W | 24773-281Y |
| R10-23 | Met film 2.2Ω 2% 1/4W | 24773-209E |
| R24 | Met film 330Ω 2% 1/4W | 24773-261D |
| R25 | Met film 2.2Ω 2% 1/4W | 24773-209E |
| R26 | Met film 2.2Ω 2% 1/4W | 24773-209E |
| R27 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R28 | Met film 330Ω 2% 1/4W | 24773-261D |
| R29-34 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R35 | Met film 4.3kΩ 2% 1/4W | 24773-288S |
| R36 | Met film 10kΩ 2% 1/4W | 24773-297M |
| R37 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R38 | Met film 10kΩ 2% 1/4W | 24773-297M |
| R39 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R40 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R41 | Met film 51kΩ 2% 1/4W | 24773-314E |
| R42 | Met film 1.0kΩ 2% 1/4W | 24773-273A |
| R43 | Met film 680Ω 2% 1/4W | 24773-269K |
| TR1 | BC208B | 28452-781A |
| X1 | Crystal oscillator, 1 MHz | 28313-871W |
| X2 | Socket, 18-way | 28488-042U |
| | Terminal post (1 of 10) | 23435-188V |
| | Handle (1 of 2) | 22324-597P |

10. **Board AM12 - Printer interface**

When ordering, prefix circuit reference with AM12

| | | |
|---|---|---|
| | Complete assembly | 44828-267A |
| C1 | Tant 22µF 20% 15V | 26486-583L |
| C2 | Cer 220pF 2% 63V | 26343-481S |
| C3 | Tant 22µF 20% 15V | 26486-230B |
| C4 | Cer 150pF 2% 63V | 26343-479W |
| C5 | Cer 150pF 2% 63V | 26343-479W |
| C6-20 | Cer 0.1µF +80-20% 100V | 26383-532E |

10. **Board AM12 - Printer interface** (continued)

| Circuit reference | Description | Code No. |
|---|---|---|
| IC1 | DC005 | 28469-405H |
| IC2 | DC005 | 28469-405H |
| IC3 | DC005 | 28469-405H |
| IC4 | DC005 | 28469-405H |
| IC5 | DC003 | 28469-403A |
| IC6 | DC004 | 28469-404Z |
| IC7 | N8T38B | 28469-175V |
| IC8 | 74LS123 | 28468-309B |
| IC9 | 74LS244 | 28469-182T |
| IC10 | 74LS00 | 28466-345H |
| IC11 | 74LS273 | 28462-615U |
| IC12 | 74LS02 | 28466-214Y |
| IC13 | 74LS74 | 28462-611A |
| IC14 | 74LS244 | 28469-182T |
| IC15 | 74LS132 | 28469-205N |
| PLA | 26-pin, $90^0$ | 23435-973N |
| R1 | Met film 330Ω 2% 1/4W | 24773-261D |
| R2 | Met film 330Ω 2% 1/4W | 24773-261D |
| R3 | Met film 330Ω 2% 1/4W | 24773-261D |
| R4 | Met film 330Ω 2% 1/4W | 24773-261D |
| R5 | Met film 680Ω 2% 1/4W | 24773-269K |
| R6 | Met film 680Ω 2% 1/4W | 24773-269K |
| R7 | Met film 330Ω 2% 1/4W | 24773-261D |
| R8 | Met film 1kΩ 2% 1/4W | 24773-273A |
| R9 | Met film 1kΩ 2% 1/4W | 24773-273A |
| R10 | Met film 22kΩ 2% 1/4W | 24773-305R |
| R11 | Met film 22kΩ 2% 1/4W | 24773-305R |
| R12-28 | Met film 2.2Ω 2% 1/4W | 24773-209E |
| R29 | Met film 470Ω 2% 1/4W | 24773-265M |
| R30 | Met film 680Ω 2% 1/4W | 24773-269K |
| | Handle | 22324-597P |

## MECHANICAL PARTS

11. Mechanical parts for the TK 1802 are given below :-

| | |
|---|---|
| Front panel, marked, TK 1802-315L version | 35903-757M |
| Front panel, marked, TK 1802-316J, -317F versions | 35902-063H |
| Top cover | 35902-058A |
| Bottom cover | 35902-079T |

11. Mechanical parts for the TK 1802 (continued)

| | |
|---|---|
| Rear panel cover | 35903-943E |
| Pivot bar | 33900-598H |
| Spring pin (1 of 2) | 21127-335X |
| Panel clips (1 of 2) | 22324-050D |
| Backplane assembly | 44990-448F |
| Boardguide (1 of 6) | 37590-210F |
| Fan (1 of 2) | 23535-104U |
| Fingerguard (1 of 2) | 23535-113G |
| Support panel assembly | 35903-941Z |

# Chapter 7

## SERVICING DIAGRAMS

CONTENTS


Para.

1 Circuit notes
1 Component values
2 Symbols
3 PCB layouts

| Fig. | | Comp. layout | Cct. |
|---|---|---|---|
| 1 | Unit A0 - Main frame wiring ... ... ... ... | - | 3/4 |
| 2 | Unit A1 - Switch panel ... ... ... ... ... | - | 5/6 |
| 3 | Unit A2 - MI/1 power supply - Input ... ... ... | - | 7/8 |
| 4 | Unit A2 - MI/1 power supply - Output ... ... ... | - | 9/10 |
| 5 | Unit A2 - MI/1 power supply - Supervisory logic ... | - | 11 |
| 6 | Board AM12 - Centronics printer interface ... ... | 12 | 13 |
| 7 | Board AA7 - LSI-11 bus terminator ... ... ... | 14 | 15 |
| 8 | Board AA7/1 - Timer/terminator - input . ... ... | 16 | 17/18 |
| 9 | Board AA7/1 - Timer/terminator - output ... ... | - | 19/20 |
| 10 | Board AA5/1 - Backplane .. ... ... ... ... | - | 21/22 |


## CIRCUIT NOTES

### Component values

1. Resistors : No suffix = ohms, k = kilohms, M = Megohms.
Capacitors : No suffix = microfarads, p = picofarads.

### Symbols

2. Symbols are to B3939 with the following additions :

Static sensitive component - see Notes and Cautions, p. iv

Test point

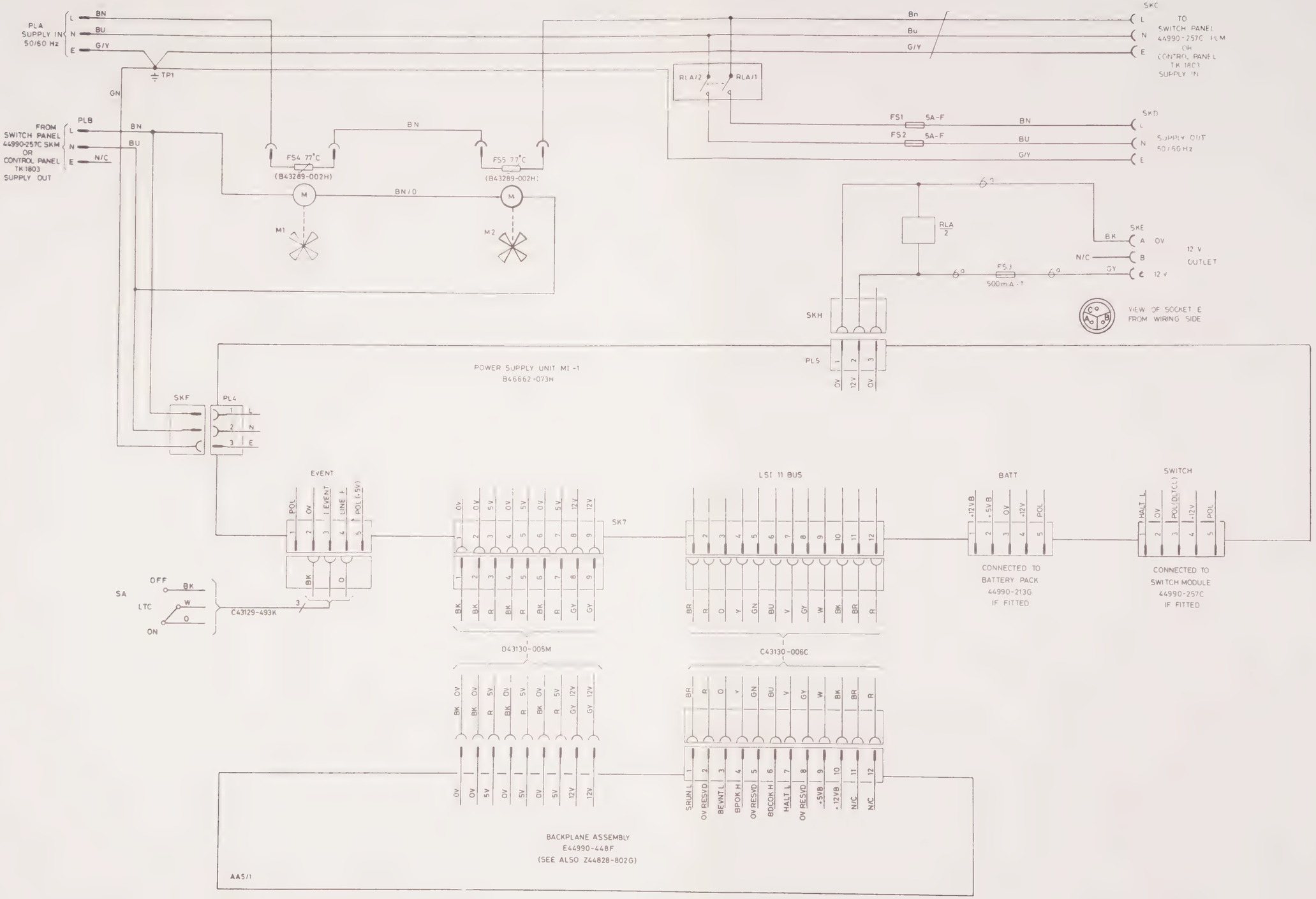
Edge connector

Ferrite bead

Unit identification

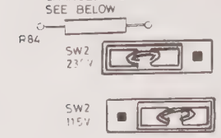
### PCB layouts

3. PCB layouts are shown as viewed from the component side.




1. FOR 115V OPERATION FANS M1 & M2 MUST BE WIRED IN PARALLEL ACROSS MAINS POWER.

LINK SW2 IN POWER UNIT MUST BE CHANGED TO THE 115V POSITION SEE BELOW




Drg. No. Z 51801-901R Sht. 1 of 1, Iss. 2

Fig. 1

Unit A0 : Main frame wiring

WIRE TYPE

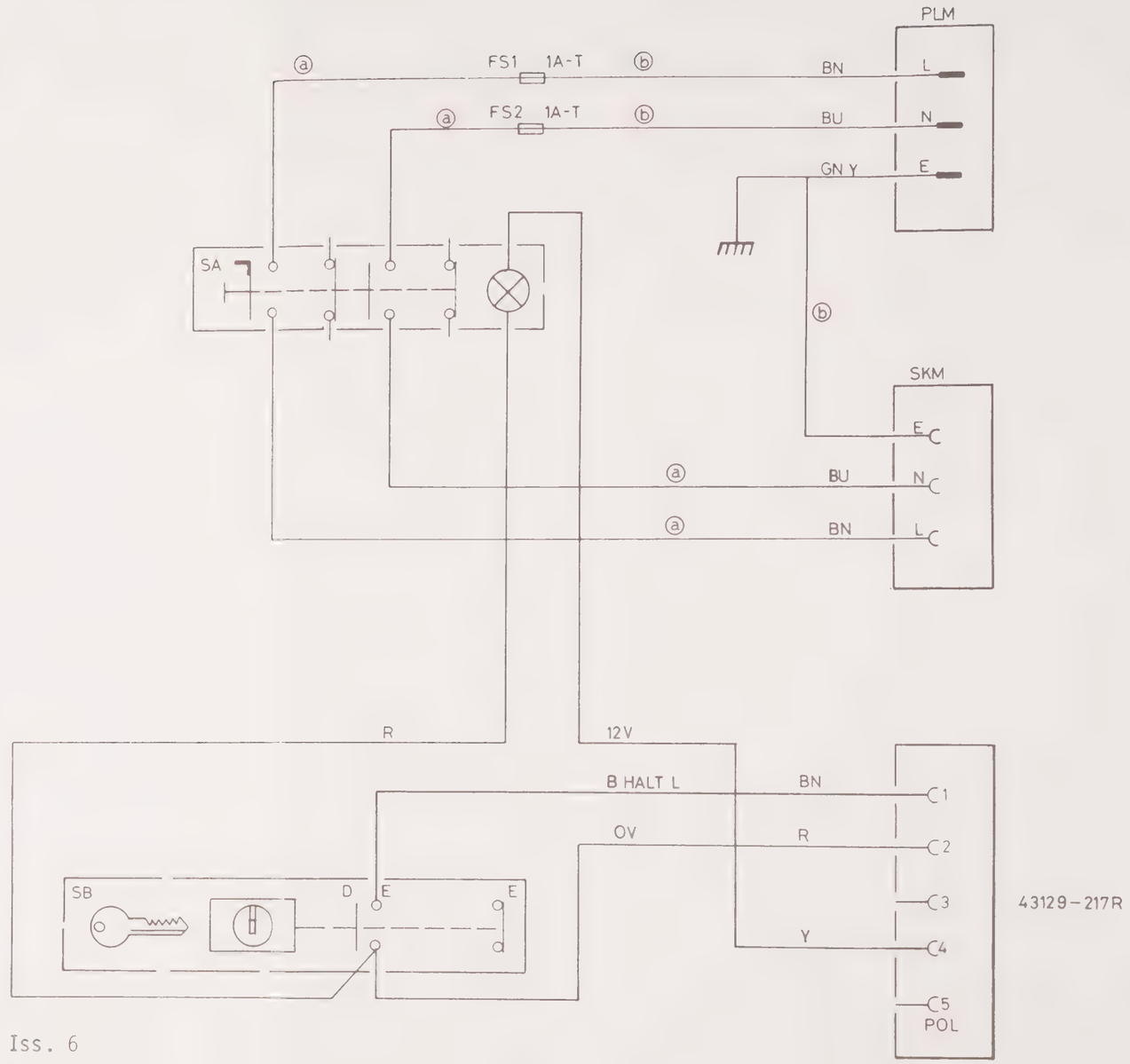
ⓐ 16/0.2

ⓑ Use wire 24/0.2

All other wires 7/0.2

COLOUR CODE

| | |
|---|---|
| BK | BLACK |
| BN | BROWN |
| R | RED |
| O | ORANGE |
| GN | GREEN |
| BU | BLUE |
| V | VIOLET |
| GY | GREY |
| W | WHITE |
| P | PINK |

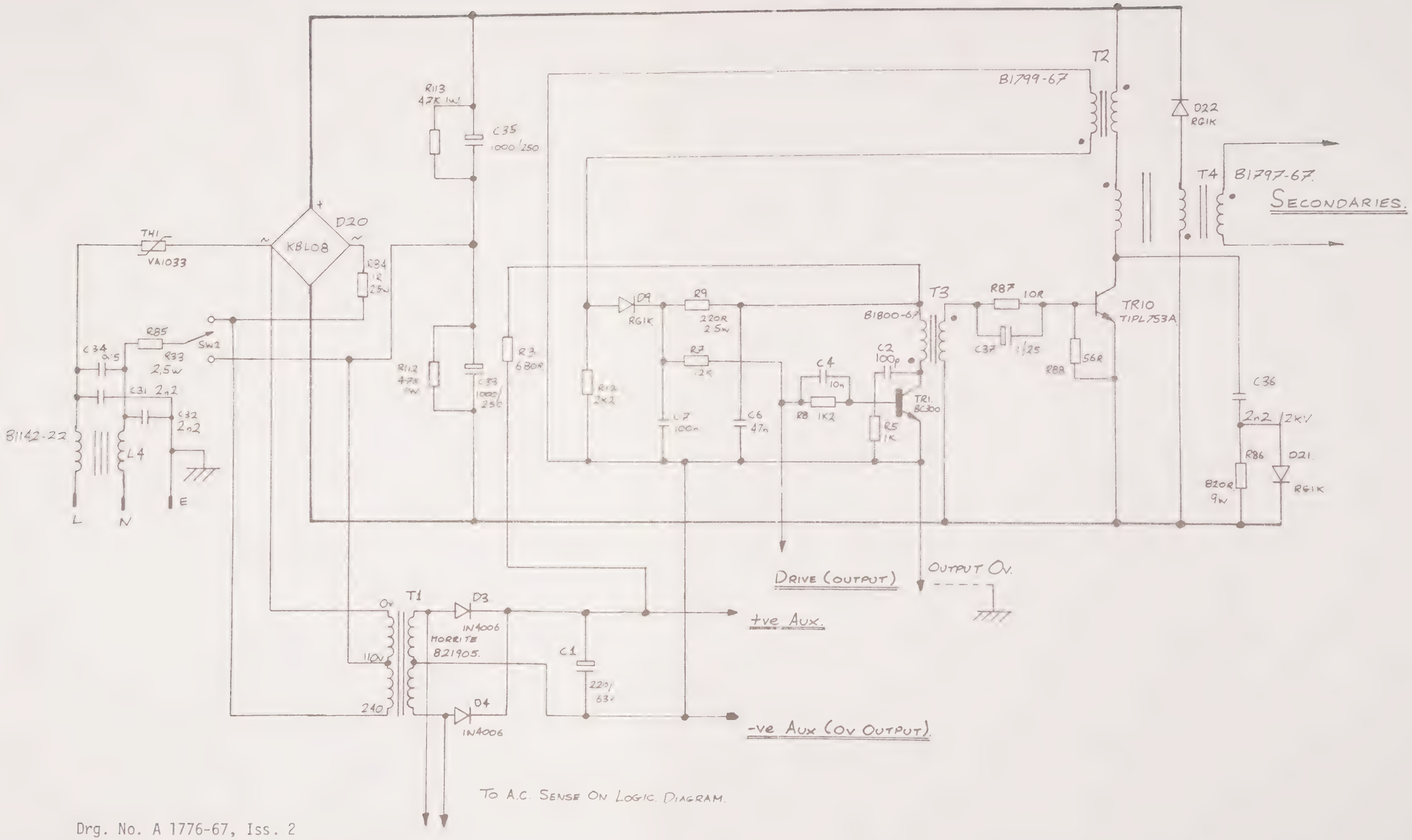



Drg. No. Z 44990-257C Sht. 1 of 1, Iss. 6

Fig. 2

May 83

Unit A1 : Switch panel




Drg. No. A 1776-67, Iss. 2

Fig. 3

Power supply unit MI/1 : Input circuit

May 83

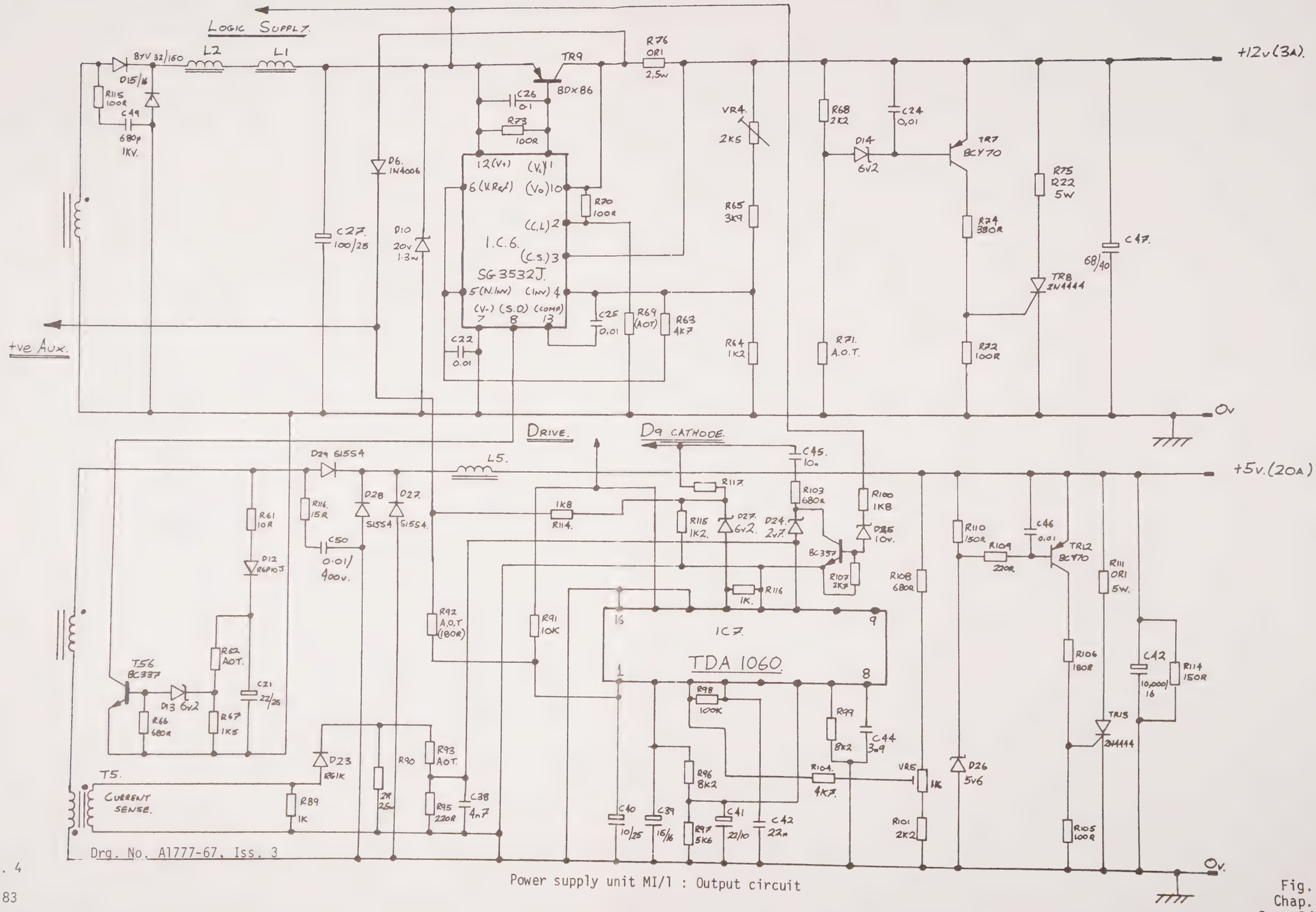
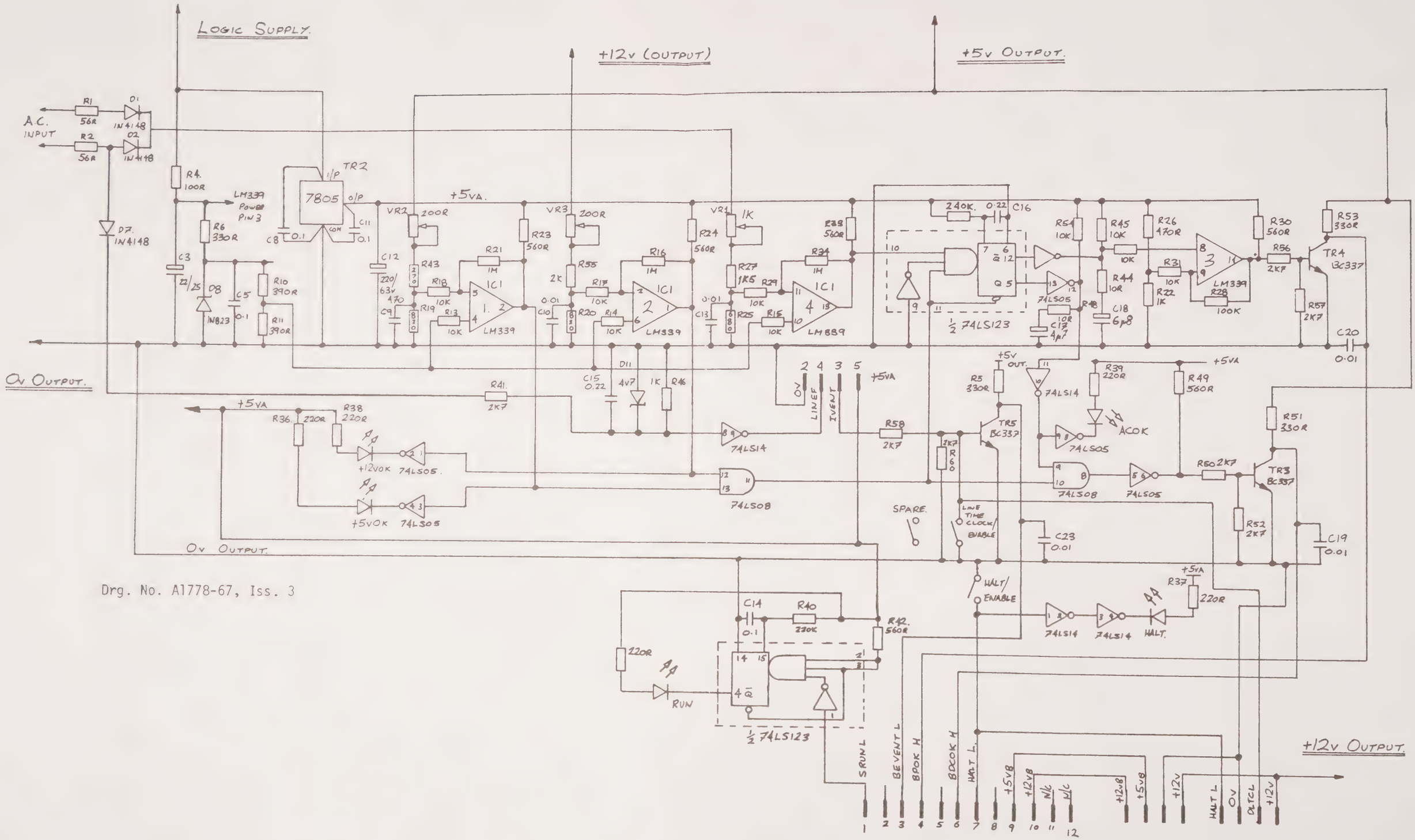



Fig. 4

May 83

Power supply unit MI/1 : Output circuit




Drg. No. A1778-67, Iss. 3

Power supply unit MI/1 : Supervisory logic circuit

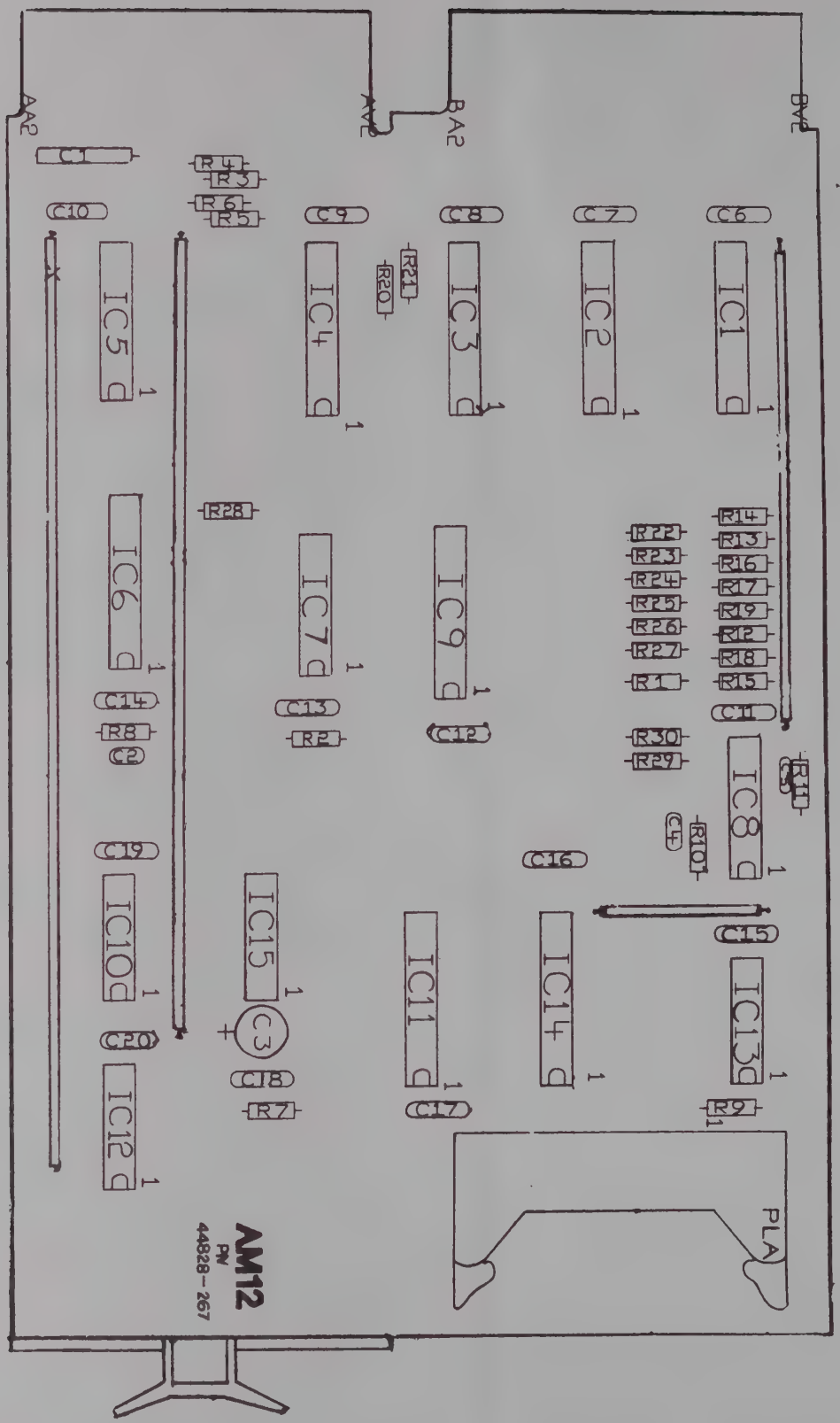



Fig. 6a Board AM12

Component layout

CONFIGURATION WHEN USED AS CENTRONICS INTERFACE

ADDRESS 177514/6 REMOVE R12,18,20
VECTOR 200 REMOVE R 22, 24-28

CONFIGURATION WHEN USED AS TICKET PRINTER INTERFACE

ADDRESS 177004/6 REMOVE R 12, 17-21
VECTOR 274 REMOVE R 22,24

Board AM12 : Centronics printer interface

Drg. No. Z 44828-267A, Sht. 1 of 1, Iss. 4

Fig. 6

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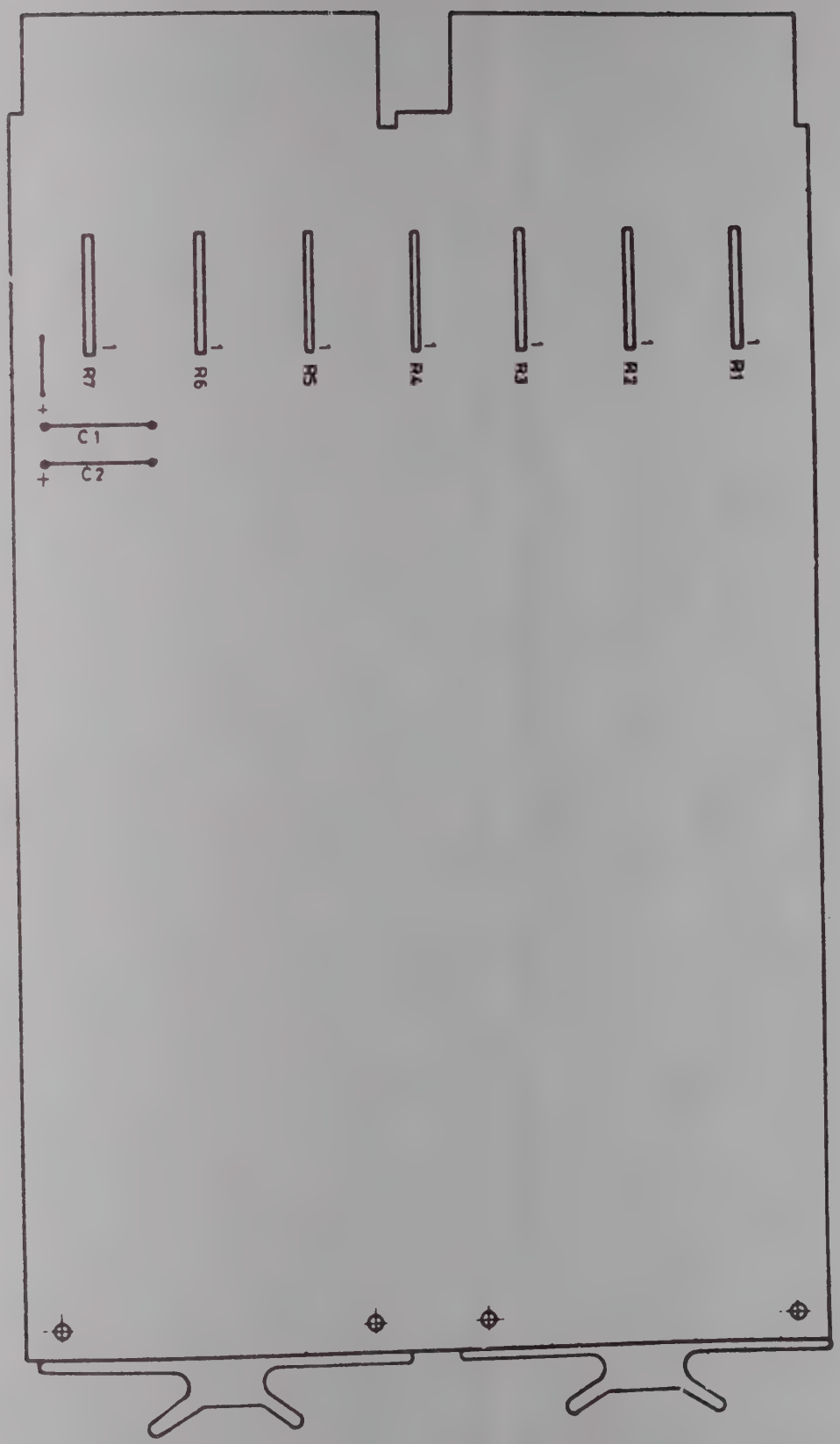
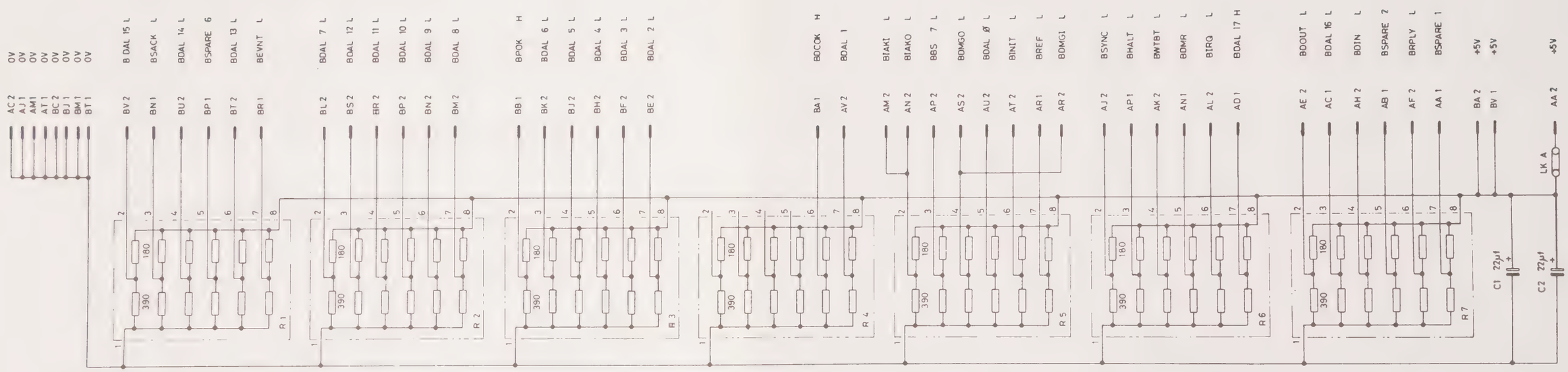



Fig. 7a Board AA7
Component layout




Drg. No. Z 44827-905Z, Sht. 1 of 1, Iss. 2

Board AA7 : LSI-11 bus terminator

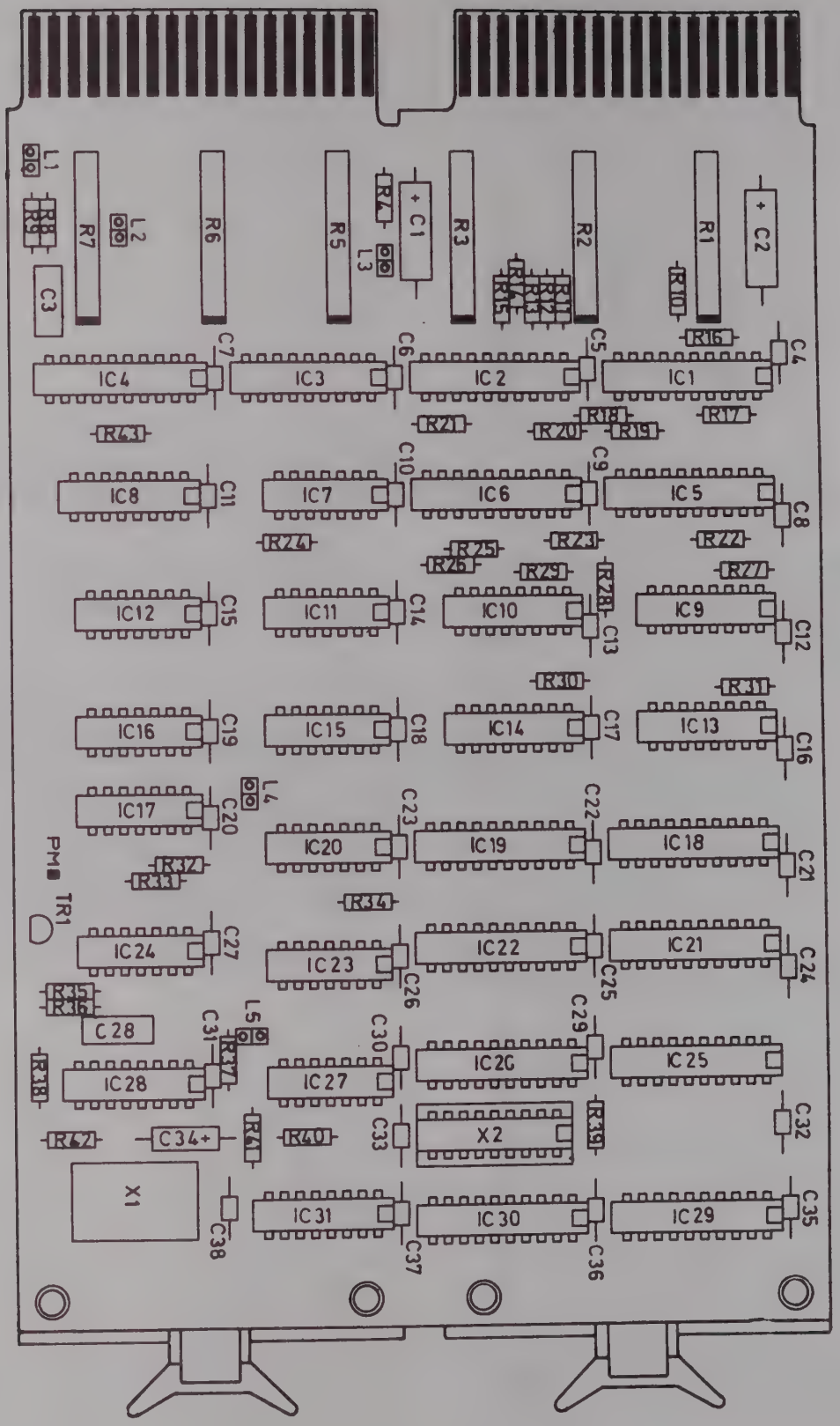
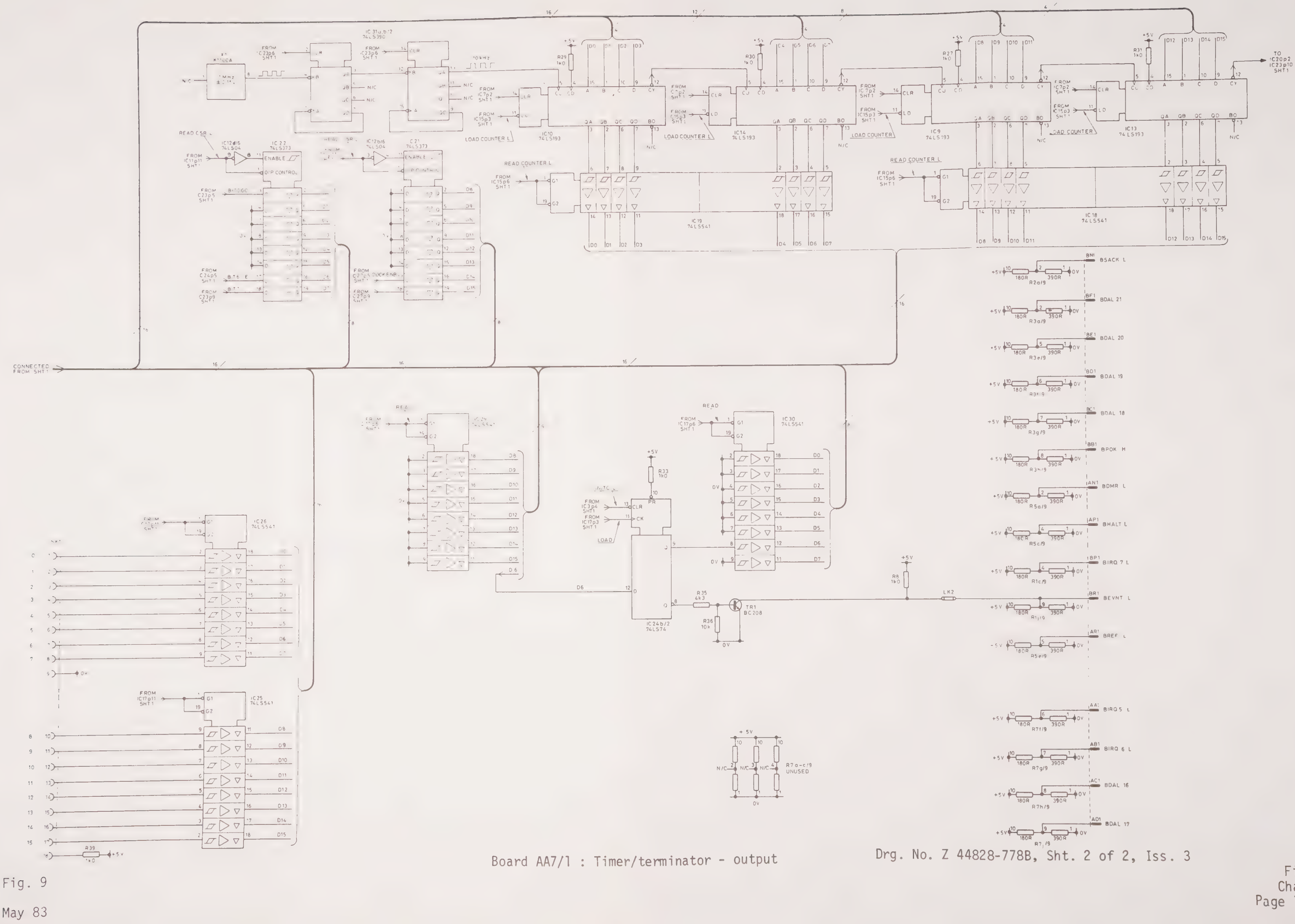



Fig. 8a Board AA7/1
Component layout

Fig. 8 Drg. No. Z 44828-778B, Sht. 1 of 2, Iss. 3

Board AA7/1 : Timer/terminator - input

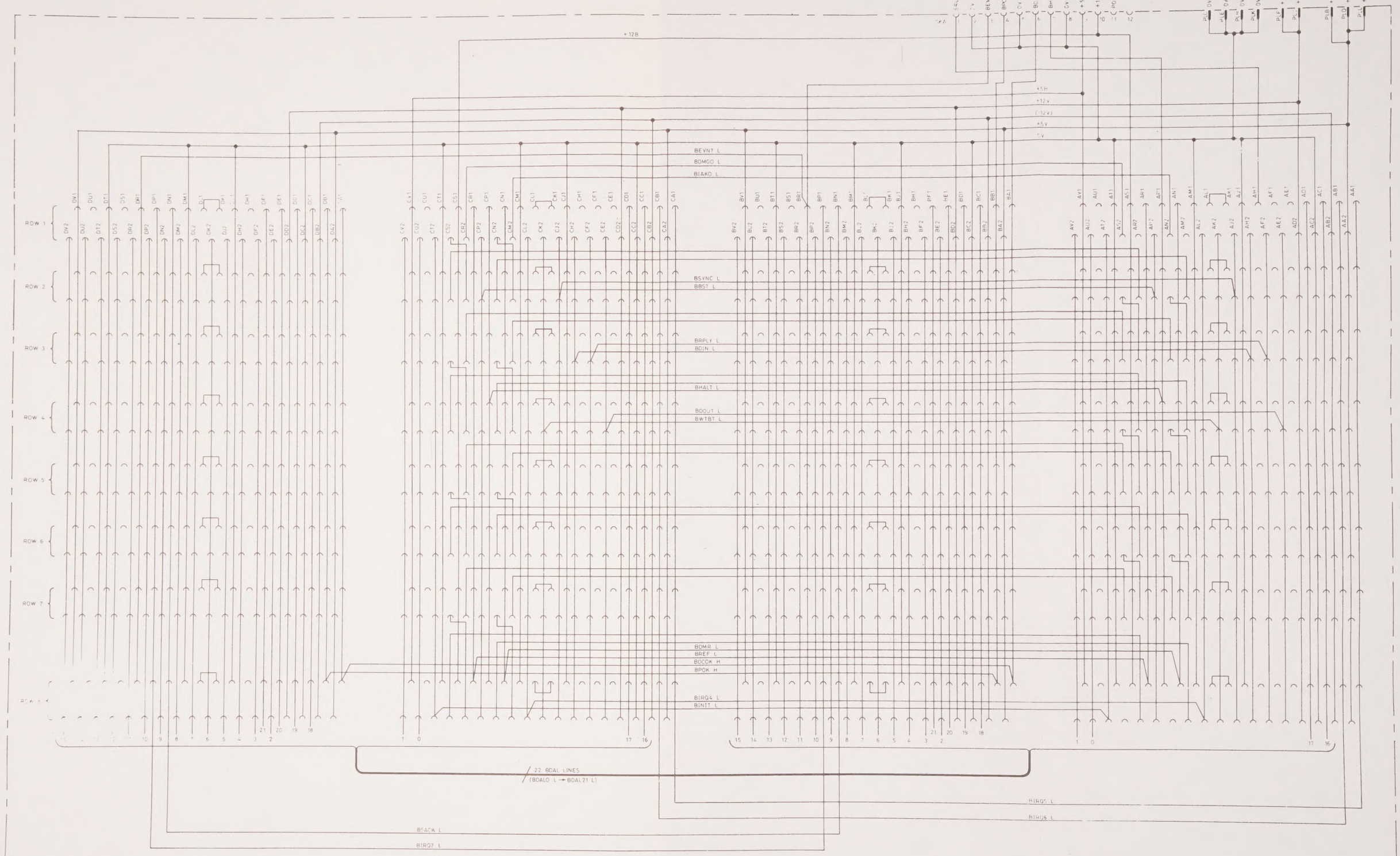



Board AA7/1 : Timer/terminator - output

Drg. No. Z 44828-778B, Sht. 2 of 2, Iss. 3

Fig. 9

May 83




Drg. No. Z 44828-802G, Sht. 1 of 1, Iss. 1

Board AA5/1 : Back plane

Fig. 10

May 83

TK 1802

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